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PHASED ARRAY ANTENNA AMPLIFIER EXPLORATORY DEVELOPMENT MODEL.(U)
AUG 79 P MUSCIANESI, J IRVINE, J RANGHELLI DAAB07-77-C-0146
UNCLASSIFIED CORADCOM-77-0146-F NL

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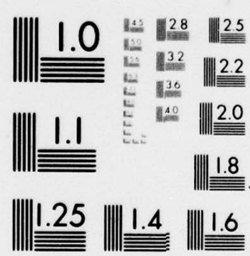

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RESEARCH AND DEVELOPMENT TECHNICAL REPORT
CORADCOM- 77-0146-F

PHASED ARRAY ANTENNA AMPLIFIER EXPLORATORY DEVELOPMENT MODEL

P. Muscianesi
J. Irvine
J. Ranghelli

ITT DEFENSE COMMUNICATIONS DIVISION
492 River Road
Nutley, New Jersey 07110

AUGUST 1979

Final Report for Period Jun 77– Jun 79

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REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER 18 19 CORADCOM-77-0146-F	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) 6 Phased Array Antenna Amplifier Exploratory Development Model.		5. TYPE OF REPORT & PERIOD COVERED 9 Final rept. June 77 – June 79
		6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) 10 P./Muscianesi J./Irvine J./Ranghelli		8. CONTRACT OR GRANT NUMBER(s) 15 DAAB07-77-C-0146
9. PERFORMING ORGANIZATION NAME AND ADDRESS ITT Defense Communications 492 River Road Nutley, N.J. 07110		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 16 17 62701A, IL762701AH92, M1, 142
11. CONTROLLING OFFICE NAME AND ADDRESS US ARMY CORADCOM ATTN: DRDCO-COM-RM-3 Ft. Monmouth, N.J. 07703		12. REPORT DATE 11 August 1979
		13. NUMBER OF PAGES 317
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office) 12 325		15. SECURITY CLASS. (of this report) Unclassified
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for Public Release; Distribution Unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Phased Array Antenna (non scanning)
C-Band Communications
Troposcatter Communications
Microwave Solid State Amplifiers
Gallium Arsenide Field Effect Transistors
LINE OF SIGHT Communications

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This final report describes the design characteristics and test results of a scale model (mechanically steerable) Phase Array Antenna Amplifier. As a result of this development investigation, a design approach for a 1 KW system is presented.

This report is prepared in two parts. The first part describes the development effort for the scale model system including specifications, design details, photographs, system diagram, test results, and trade off analyses. The second part of this report covers the design approach selected for a 1 KW system. This design approach

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is based upon the technical accomplishments resulting from the scale model development.

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TABLE OF CONTENTS

TABLE OF CONTENTS (CON'T)

I. INTRODUCTION

This final report describes the design characteristics and test results of a scale model (mechanically steerable) Phased Array Antenna Amplifier. As a result of this development investigation, a design approach for a 1 KW system is presented.

This report is prepared in two parts. This first part describes the development effort for the scale model system including specifications, design details, photographs, system diagram, test results, and trade off analyses. The second part of this report covers the design approach selected for a 1 KW system. This design approach is based upon the technical accomplishments resulting from the scale model development.

II. EXPLORATORY DEVELOPMENT SCALE MODEL

II-A. OBJECTIVES

The objective of this exploratory development scale model program was to demonstrate the cost and technical feasibility of a (non-electronic scanning) solid state phased array transmit/receive antenna amplifier. This system employs distributed solid state amplifiers and highly efficient low voltage power supplies to increase the reliability of tactical troposcatter communications. A failure would then be characterized by a gradual reduction in ERP as individual amplifier modules fail as opposed to catastrophic communications outage. The primary goal of this program is to develop design information and tradeoff analyses culminating in a design concept for a low cost, reliable, high power (1 kw) solid state phased array antenna amplifier system for tactical deployment.

II-B. DESCRIPTION

The phased array antenna amplifier is an integration of many low power solid state, amplifier modules with transmit and receive antenna arrays forming a complete power amplifier/antenna unit. The antenna provides for duplex operation of transmitter and receiver simultaneously (using cross polarized signals).

The developed scale model is approximately one-tenth in size and 1/100th in power output of a full 1 kw, 100 square foot aperture, phased array antenna amplifier.

The solid state phased array power amplifier is intended to be used in conjunction with military tactical troposcatter radio sets to improve the reliability of these communication links. The scale model developed under this program was designed to interface with the AN/GRC-143 army standard tactical troposcatter radio.

The investigation emphasized efficient, reliable, low cost techniques for achieving the objective. The relative importance of major factors considered are as follows:

- Minimum cost per solid state amplifier module
- Power output and gain
- Reliability
- Broadband operation over the 4.4 - 5.0 GHz military band
- Minimum size and weight
- Maximum power efficiency

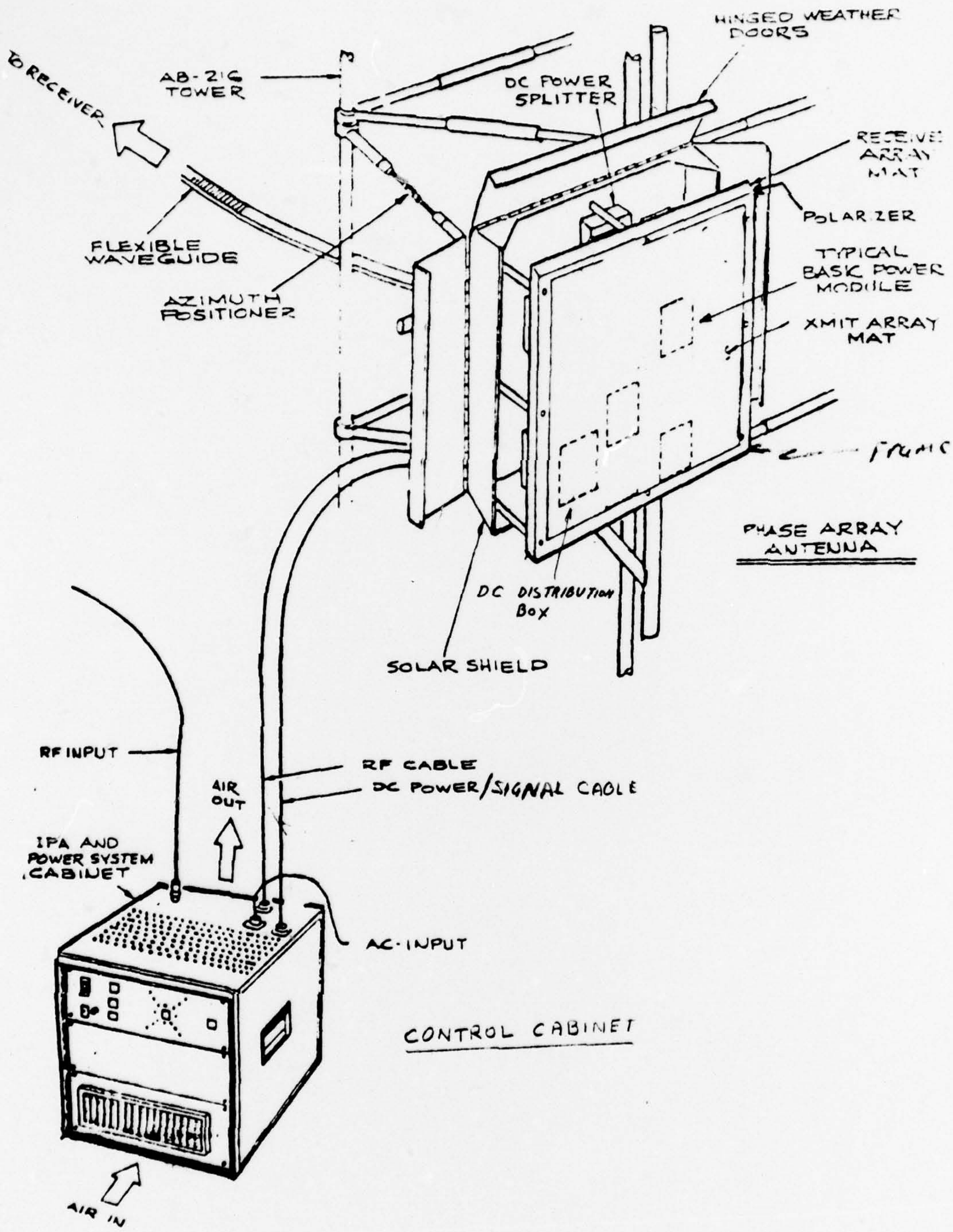
II-C. PROGRAM SCHEDULE

The exploratory development program was started in June 1977 and the completed scale model delivered to USA CORADCOM, Ft. Monmouth, NJ, in June 1979.

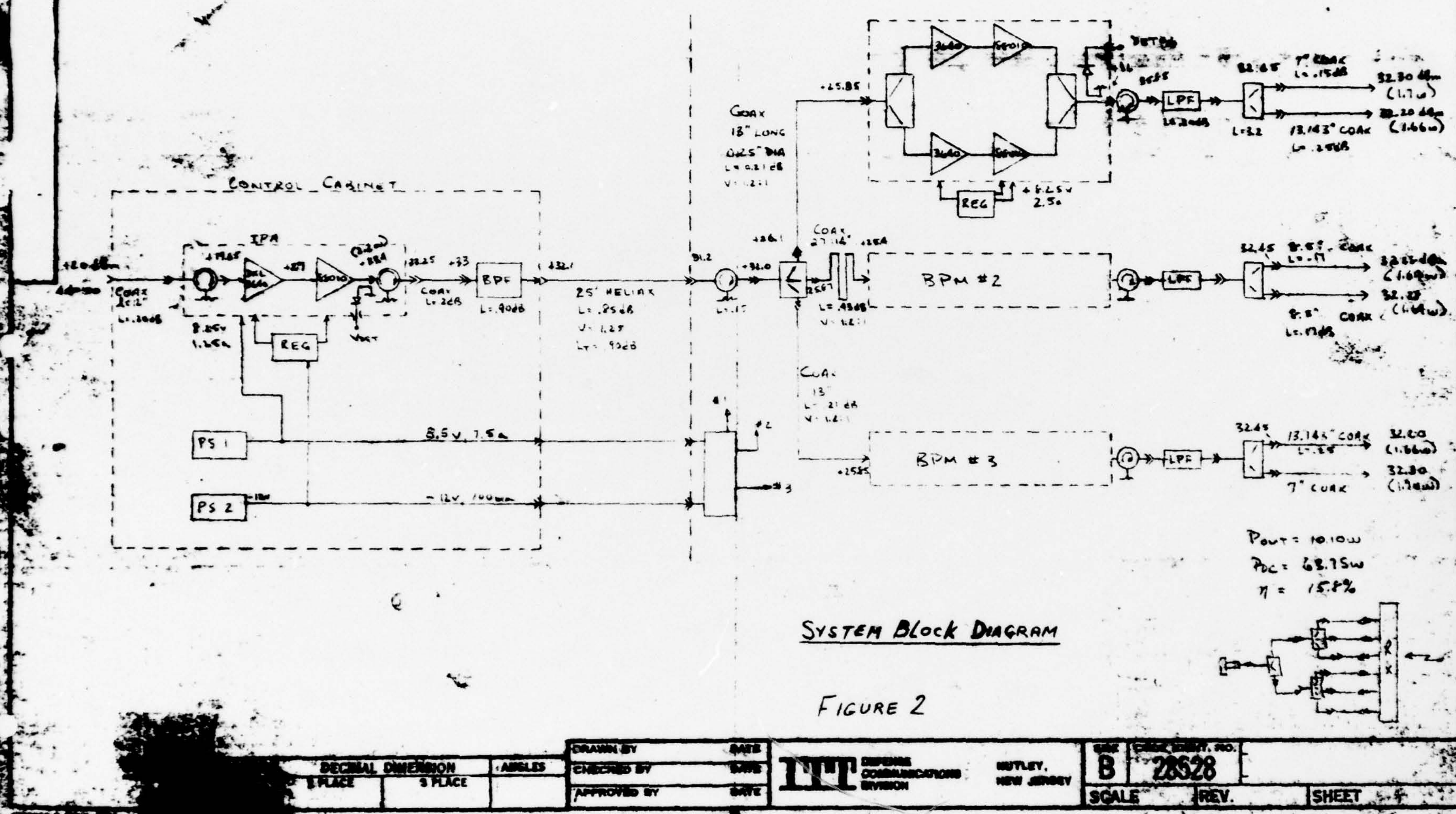
II-D. SYSTEM DESCRIPTION

The scale model Phased Array Antenna Amplifier system consists of a transmitter amplifier matrix and antenna array, and a receiver antenna array which operates over the full 4.4 - 5.0 GHz frequency range. The system pictorial is shown in Figure 1, and the system block diagram is shown in Figure 2. Figures 3 thru 9 show the system at various levels of assembly.

The transmitter matrix consists of an Intermediate Power Amplifier (IPA) mounted in the control cabinet which provides the RF drive for 3 parallel amplifiers, Basic

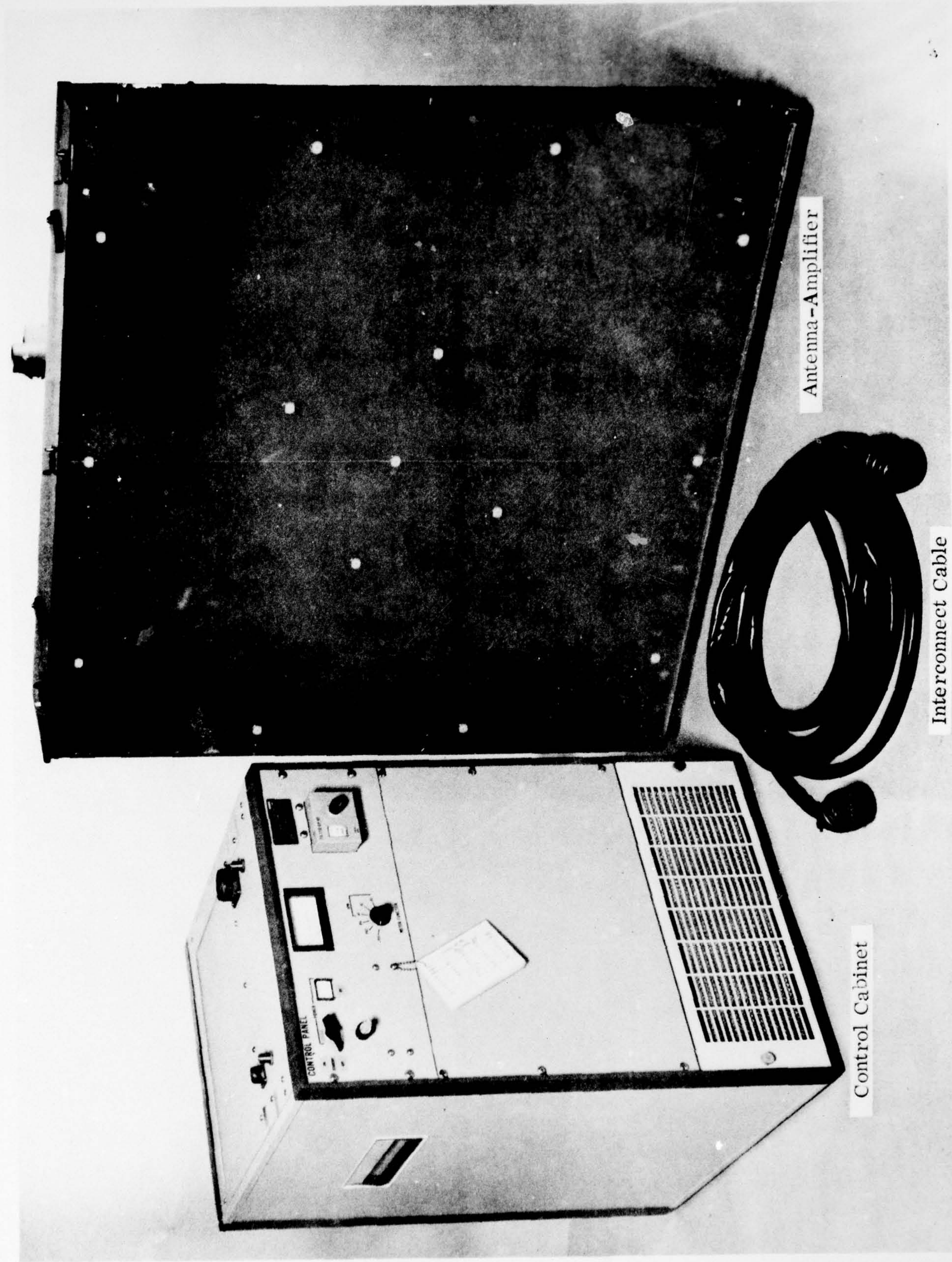


- FIGURE 1 SYSTEM PICTORIAL -

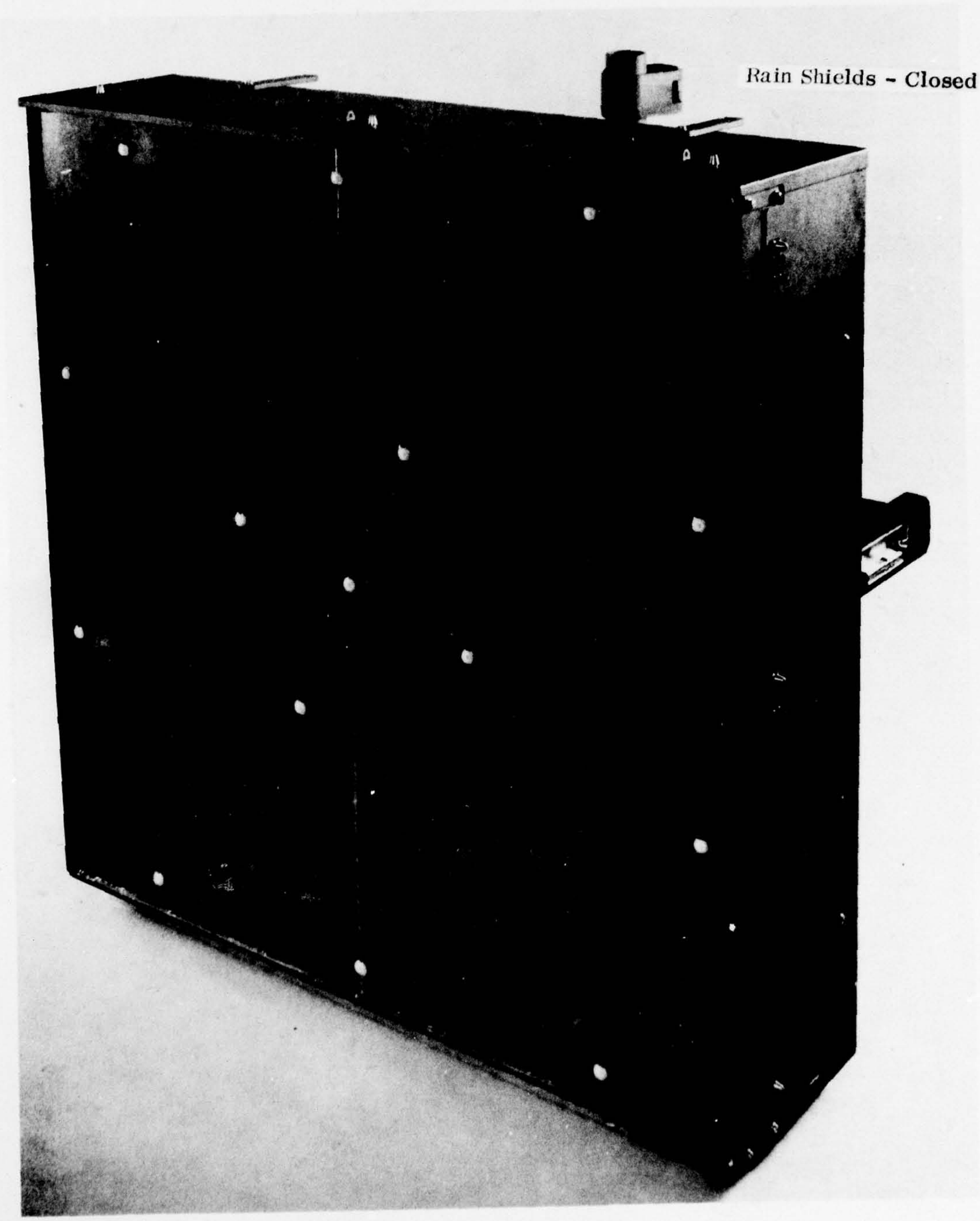


SYSTEM BLOCK DIAGRAM

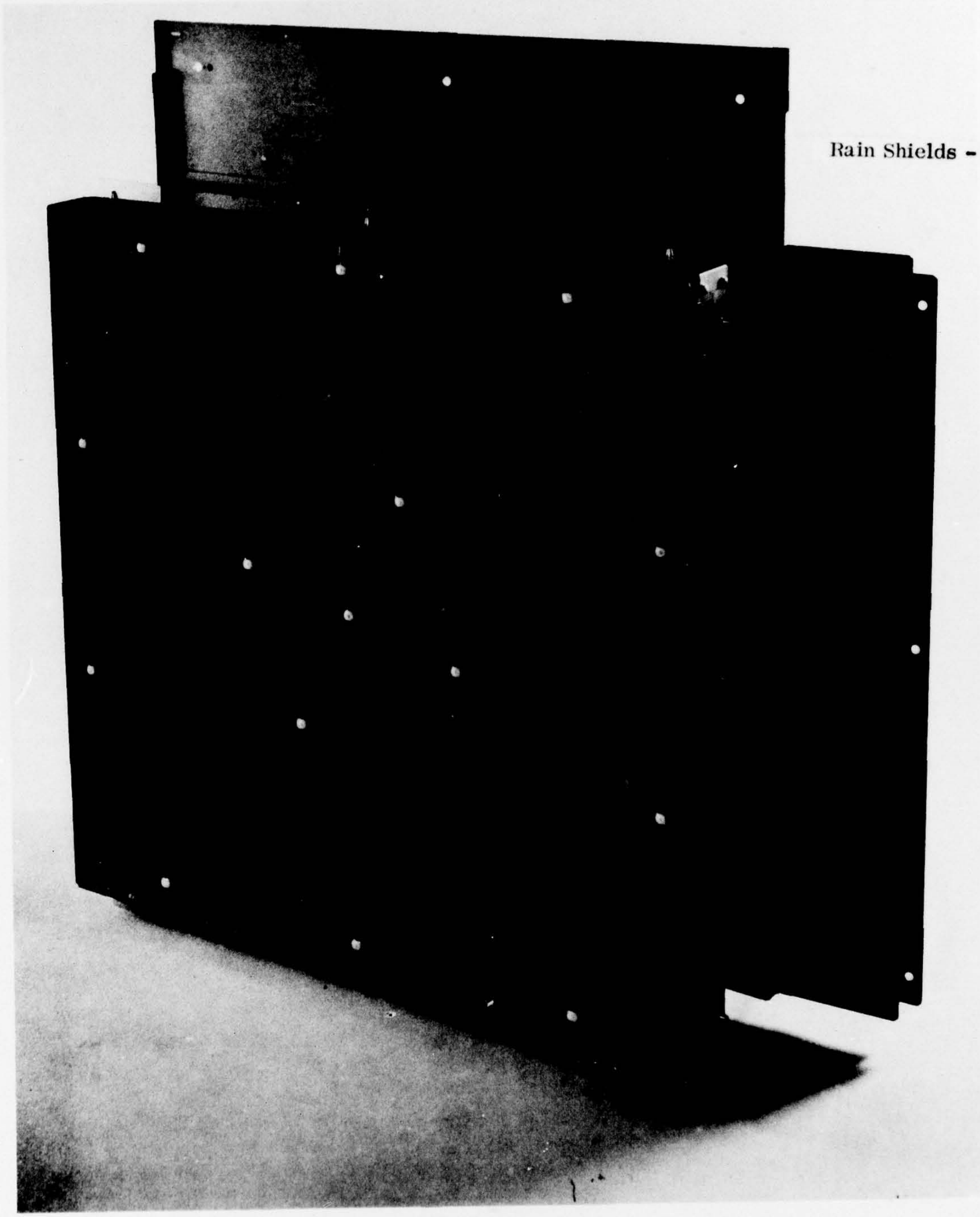
FIGURE 2



Scale Model - Phase Array Antenna Amplifier

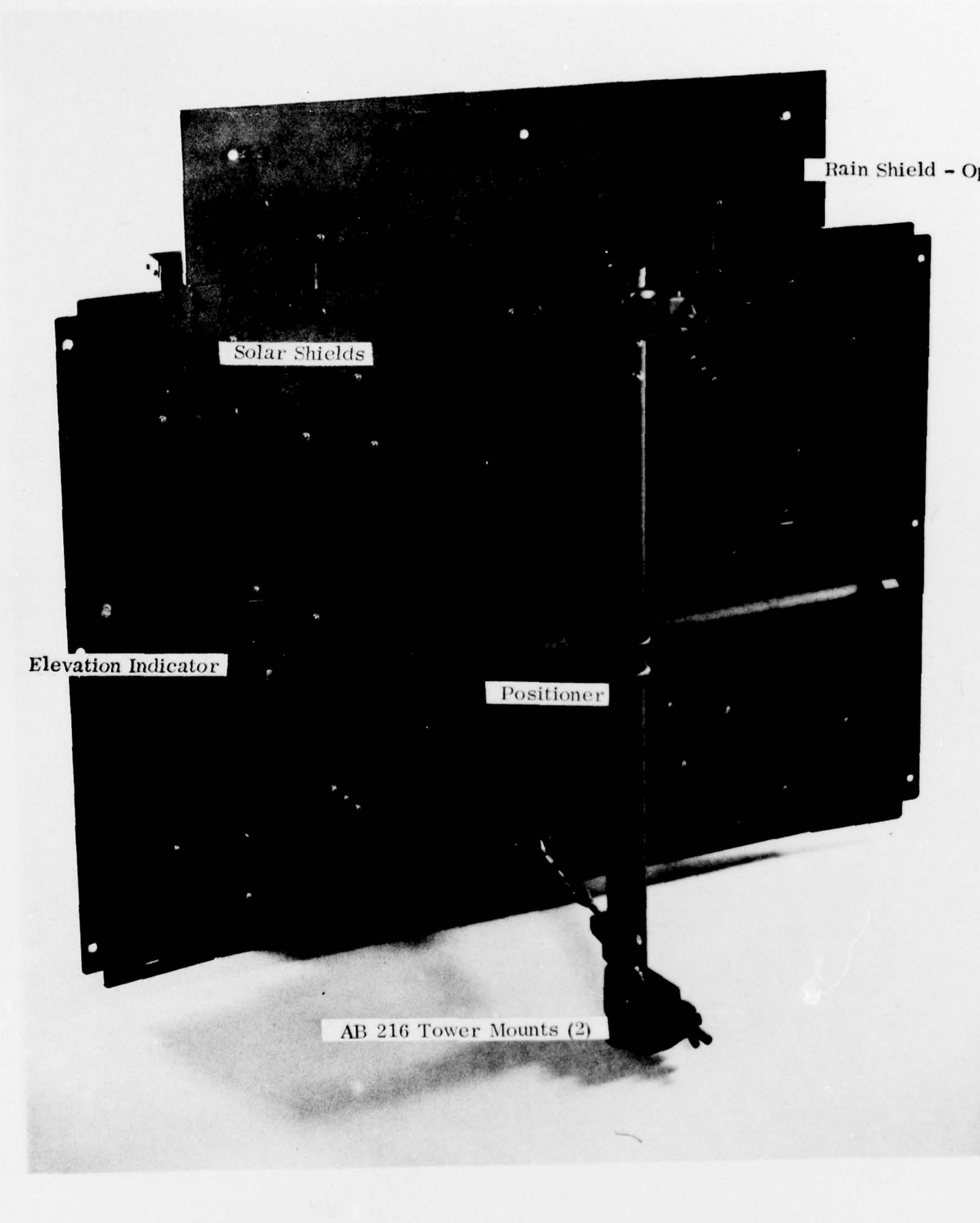


Antenna Amplifier

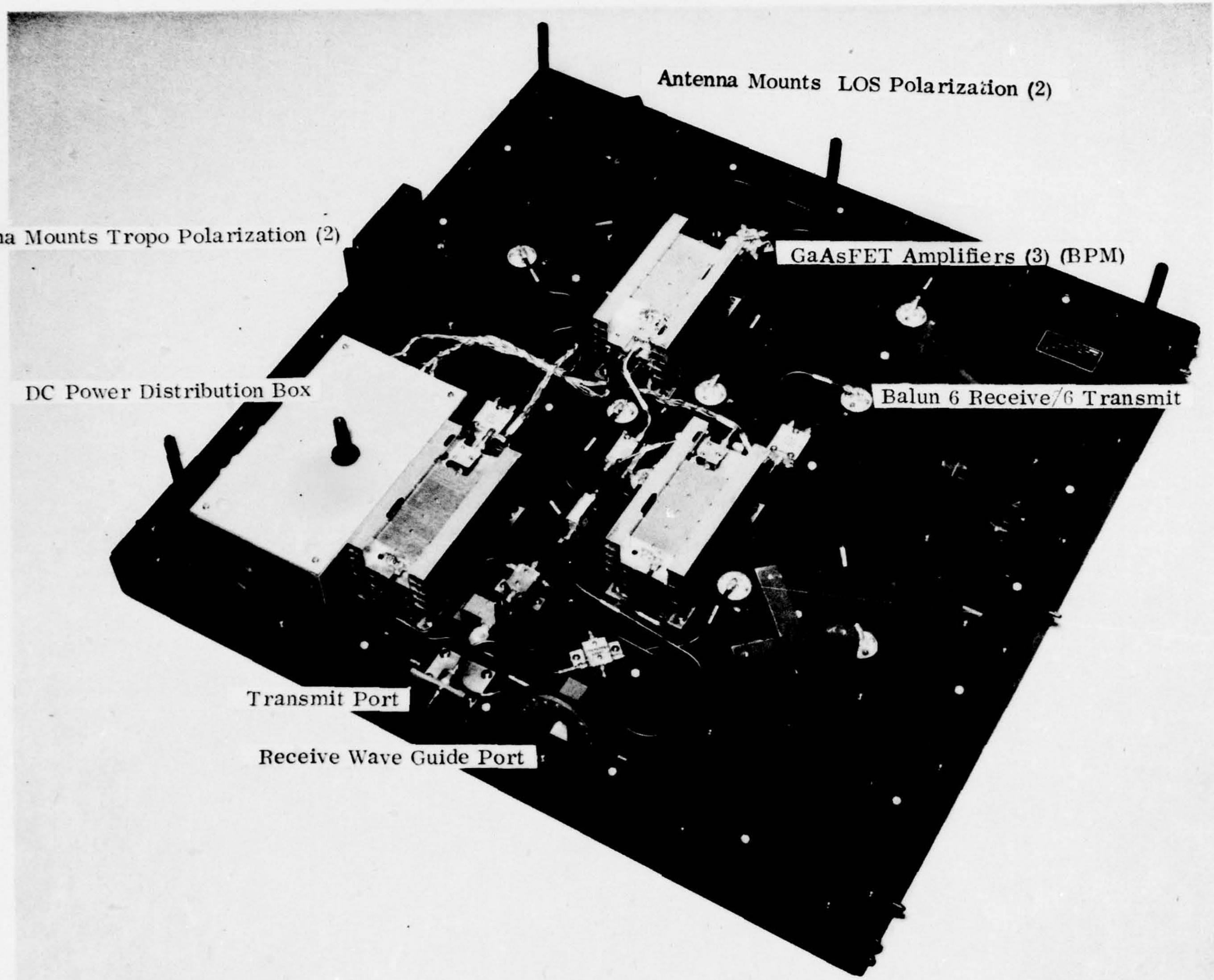


Rain Shields - Open

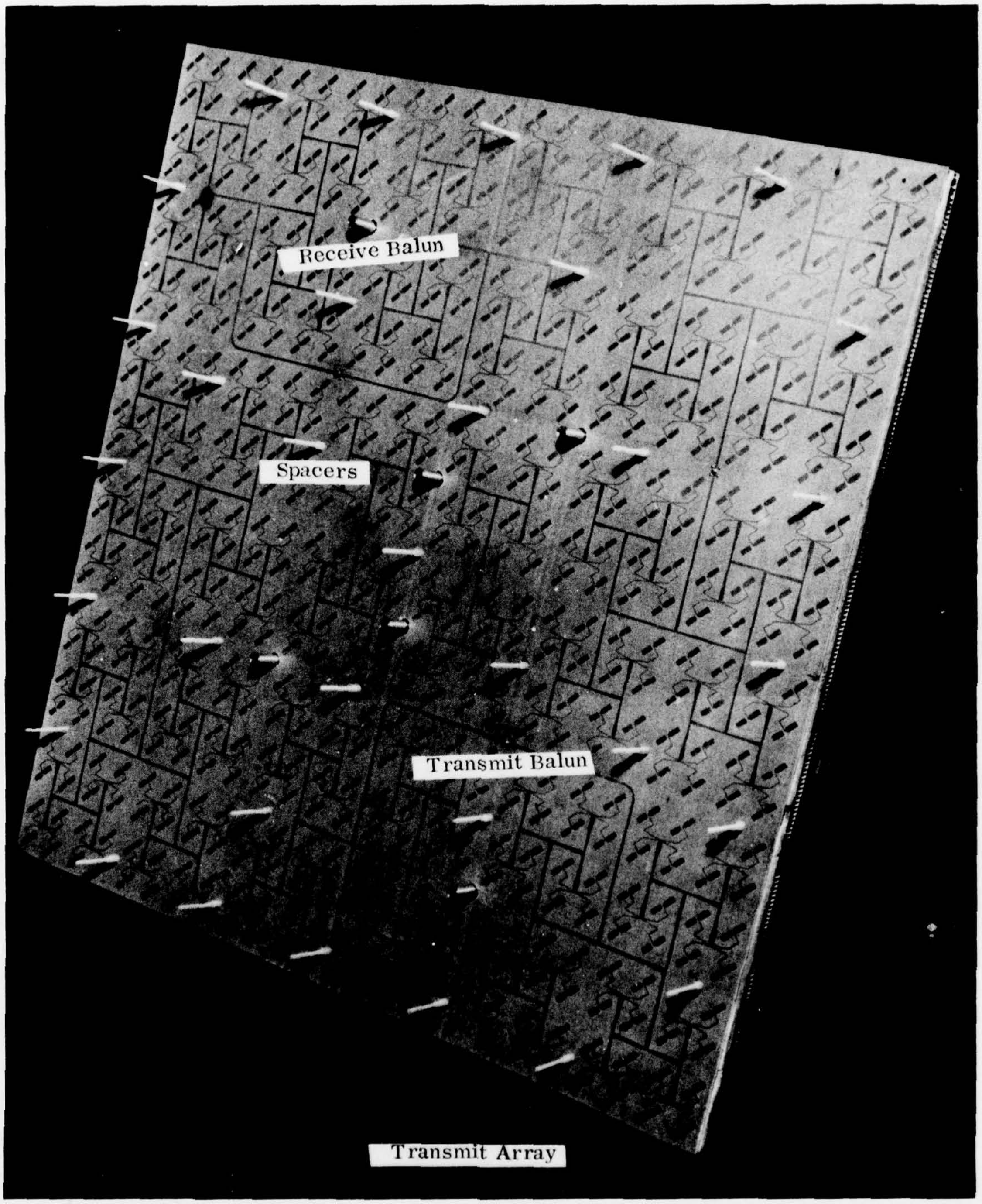
Antenna Amplifier



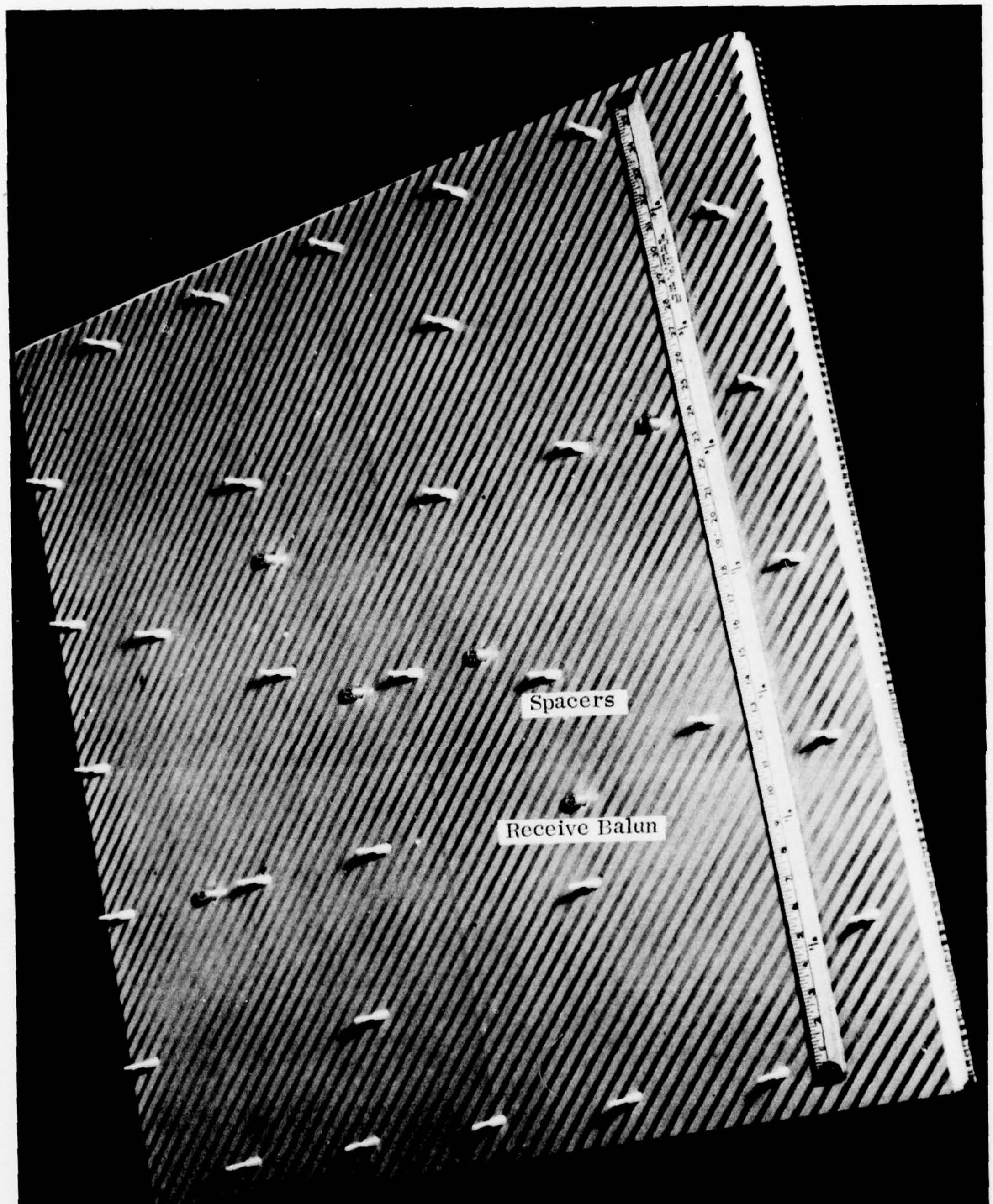
Antenna Amplifier - Back View



Antenna Amplifier - Back View, Solar Shield Removed



Printed Antenna Laminate



Printed Transmit Ground Plane Laminate (Polarizer)

Power Modules, (BPM's) mounted directly in back of the antenna array. These 3 BPM's provide a nominal 4 watts each. The transmit array spatially adds the 3 BPM individual power outputs to obtain the total array output power of 12 watts. An antenna array gain of 30 dBi provides the +70 dBm effective radiated power. Both the IPA and BPM's use GaAsFET amplifier devices.

The RF input to the system is a minimum 100 mw in the 4.4 - 5.0 GHz band provided by the (exciter of the) AN/GRC-143 radio set. An isolator is provided on the input to the IPA to meet the system input VSWR spec of 1.5:1. The IPA output is detected, and the voltage is used to drive a front panel meter providing the operator with a visual indication of the IPA status. A single knob tunable four pole band pass filter follows the IPA and is provided to minimize the noise contribution to the AN/GRC-143 receiver from the IPA and AN/GRC-143 transmitter. An isolator with high power load is included in the IPA to protect the output transistor from power reflected from the bandpass filter when the filter is not tuned to the radio transmitter frequency.

The RF equipment discussed so far is mounted in a control cabinet, together with power supplies and Built In Test Electronics (BITE) circuitry. A 25-foot coax cable is provided to take the RF output from the BPF in the control cabinet up to the antenna amplifiers. An isolator is provided at the input to the antenna amplifier matrix to provide a good terminating impedance for the 25-foot cable and thus assure a good VSWR at the bandpass filter. A 3-way power divider then splits the power into 3 equal amplitude, equal phase signals. Each BPM (Basic Power Module) has a nominal 11 dB gain over the full band. An RF detector in the output of each BPM is used to drive the BITE circuitry and provide an indication of the amplifier status at the control cabinet front panel. A low pass filter with a cut-off frequency of 5.15 GHz and a minimum of 50 dB attenuation at frequencies greater than 8.8 GHz follows each BPM to attenuate 2nd harmonics before reaching the antenna array.

The antenna consists of orthogonal transmit and receive arrays, each with its own ground plane (Figure 10). Each array design is identical in terms of the number of dipoles and amplitude taper but the arrays are assembled orthogonally. The transmit array has 6 feeds, 2 for each of the 3 BPM's. The output of each BPM is split by a two way hybrid. The typical gain of the transmit antenna is 31.0 dB resulting in a typical ERP of +70 dBm. The sidelobe amplitude of the array is -15 dB. The receive array has a slightly lower gain due to the fact that this array is positioned behind the transmit array and has a more complex feed arrangement. Some of the receive power combining is performed in the array, resulting in 6 outputs, which are then combined by 2 way and 3 way hybrid summers resulting in one output for the AN/GRC-143 receiver. The sidelobe amplitude of the receive array is -15 dB.

The system is powered from two DC power supplies located in the control cabinet. The first power supply is a 10 V, 15 amp unit while the second is a 12 V, 1 amp unit. The 10 V supply provides the positive voltage for the GaAs FET devices' drain while the 12 V supply provides the negative voltage for the GaAsFET gates. A DC power distribution cable carries the 8.0 amps required for the antenna BPM's. Remote sensing of the positive (10 V) DC voltage at the antenna distribution box assures a constant operating voltage for the BPM's. The BITE circuitry monitors the status of the DC power supplies. Each BPM has an RF detector which provides control panel indication of the antenna BPM's activity status.

II E. System Performance

A summary of System Performance is included on pages 14 - 16.

II-F. SYSTEM DESIGN AND DISCUSSION

Development of the scale model system required investigation into two main technical areas:

- Matstrip Duplex Antenna Design (Printed Array)
- 'C' Band (4.4 GHz - 5.0 GHz) Solid State High Power Generation and Distribution.

SCALE MODEL SYSTEM PERFORMANCE - SUMMARY △

PARAMETER	PERFORMANCE	REQUIREMENT
Amplifier Matrix		
Frequency Range	4.4 - 5.0 GHz	4.4 - 5.0 GHz
1dB Bandwidth	4.4 - 4.95 GHz - 1.5dB@ 5 GHz	4.4 - 5.0 GHz
Power Input	100 mW Minimum	100 mW Minimum
Power Output	7.14 w Minimum	10 w Minimum
DC-RF Efficiency	13.4% Minimum Typically $>$17%	14% Minimum
ERP	69.5 dBM Minimum 71.9 dBM Maximum	70 dBM Minimum
Spurious Radiation (including Harmonics)	-88 dBC Maximum	-80 dBC Maximum
Parasitic Oscillation	None	None
Prime Power	155 Watts	1000 Watts Maximum

△ **See Appendix A for Details**

SCALE MODEL SYSTEM PERFORMANCE - SUMMARY △

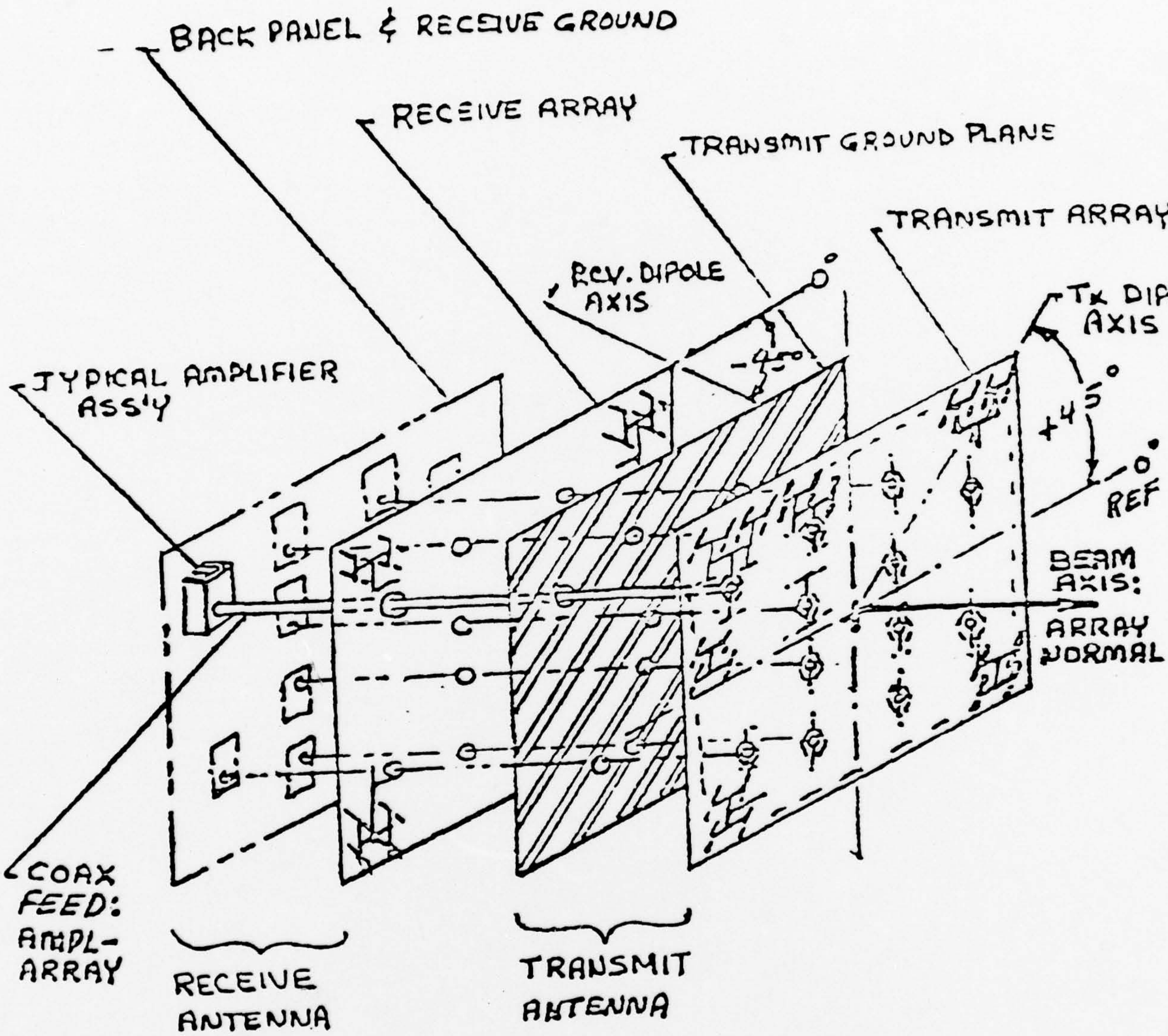
PARAMETER	PERFORMANCE	REQUIREMENT
Size	Antenna Array: Aperature - 9.96sq ft Including frame 10.56sq ft	Antenna Array Area not to exceed 10 sq ft
	Control Cabinet 30H x 21W x 17D	None
Weight	Antenna Array 120 lb Control Cabinet 98 lb Interconnect Cables 26 lb 244 lb	Minimal
Structural Interface	AB-216 Tower	AB-216 Tower
Input Connector	Type N, Stainless Steel	Type N
Output Connector	WR-187 with UG/149 Flange	WR-187 with UG/149 Flange
Cooling	Antenna Array (includes Amplifiers) - Convection Cooling Control Cabinet - Forced Air Cooling	Air Cooling
Mechanical Positioning	Azimuth $360^o \pm .5^o$ Elevation $5^o \pm .2^o$	Azimuth $360^o \pm .5^o$ Elevation $5^o \pm .2^o$
Antenna Gain	Transmit 29.6 Min, 32.5 Max Receive 27.9 Min, 30.5 Max	Transmit 30dbi Minimum Receive 30dbi Minimum
Antenna Beam Width	Transmit 3.8^o Maximum Receive 3.9^o Maximum	Transmit 5^o Maximum Receive 5^o Maximum

△ See Appendix A for Details

SCALE MODEL SYSTEM PERFORMANCE - SUMMARY Δ

PARAMATER	PERFORMANCE	REQUIREMENT
Duplex Operation	No measurable Receiver Noise Figure Degradation	AN/GRC Receiver Noise Figure Degradation not greater than 1.5 dB with 100 MHz TX-RX separation
Antenna Polarization	Troposcatter Polarization Transmit + 45° WRT Horizon Receive - 45° WRT Horizon	Troposcatter Polarization Transmit + 45° WRT Horizon Receive ± 45° WRT Horizon
	Line of Sight Polarization Transmit 90° WRT Horizon Receive 0° WRT Horizon	Line of Sight Polarization not required
Sidelobes	Transmit Array w/o Amplifiers E-Plane 14.9 dB H Plane 15.0 dB Intercardinal Plane 20 dB	15 dB Maximum
	Receive Array E Plane 15.8 dB H Plane 14.1 dB Intercardinal Plane 17.3 dB	
Antenna Array VSWR	Transmit 1.51:1 Minimum 2.31:1 Maximum Receive 1.86:1.0	1.50:1.0
VSWR - System Input	1.36:1.0	1.50:1.0

Δ See Appendix A for Details



ANTENNA MATRIX CONSTRUCTION

FIGURE 10

Previous programs at ITTDCD developed circularly polarized printed dipole antenna array for 'X' band (8 GHz) application. These programs were:

- Advanced Satellite Communication Antennas, Contract No. DAAB07-68-C-0018 performed for the U.S. Army Satellite Communications Agency, Fort Monmouth, New Jersey.
- Antenna AS-2614 (XN-2)/BRA-35, Contract No. N00024-70-C-1422 performed for the Department of the Navy, Naval Ship Systems Command, Washington, D.C.

In order to adapt this technique for the phased array program, the following details had to be addressed:

- Scaling 'X' Band dipole design to 'C' band
- Generating a computer program to evaluate antenna performance for various amplitude tapers
- Investigate laminate materials for best performance
- Analyze design to determine if a single laminate layer could simultaneously satisfy receive and transmit requirements
- Evaluate trade off between a one piece construction (for laminate) or a sectionalized construction
- Locate vendor capable of processing a large laminate.

For the Solid State RF power generation and distribution, several key areas had to be investigated. These areas are:

- Choice of a semiconductor devices to meet the systems needs
- Choice of substrate material and bonding techniques
- Phase and amplitude characteristics of power dividers
- Low loss distribution of RF power from the IPA to the antenna amplifiers and from antenna amplifiers to antenna baluns. (Isolators, low pass filters, cable, etc.)
- Methods of combining (splitting) Class 'C' power transistor to minimize interstage interface problems
- Determining effects of amplifier noise and gain on co-located receiver.

II F.1 ANTENNA DESIGN

This section will provide the details of the antenna design including mechanical description, trade off analyzes, laminate material comparison, computer aided design .

II F.1A MECHANICAL DESCRIPTION

Figure 11 shows the assembly drawing of the scale model antenna amplifier followed by a parts list - pages 20 thru 22.

The antenna structure consists of 3 printed laminates items 6, 7 and 8 of view C-C. Item 5 is the aluminum honeycomb ground plane which provides the main mounting member. This aluminum honeycomb is light weight, easy to work, and very stiff. Threaded inserts, available from Shure Lok, are installed in the Honeycomb and used to mount all components to this ground plane. View C-C also shows the transmit balun items 14, 16 and 17. Item 10 is the foam dielectric spacer and item 12 is the nylon spacer. The function of these two elements is to insure proper spacing between antenna laminates, and (item 13) to secure the laminates to the aluminum honeycomb (item 5).

The mechanical design provides mounting for Army Standard Troposcatter and Line-of-Sight antenna polarization compatability by selecting either the horizontal mounting (as shown) or the 45° rotation (clockwise) items 41 and 42.

About the perimeter of the antenna assembly, doors are provided to protect the RF components during inclement weather. View D-D shows the side door in the closed position, with the latch secured to the side frame (item 35). Item 39 is the latching arm which engages the thumbscrew (item 50, P/O solar shield item 38) to hold the side door in the open position. A similar door is provided at the top of the antenna assembly.

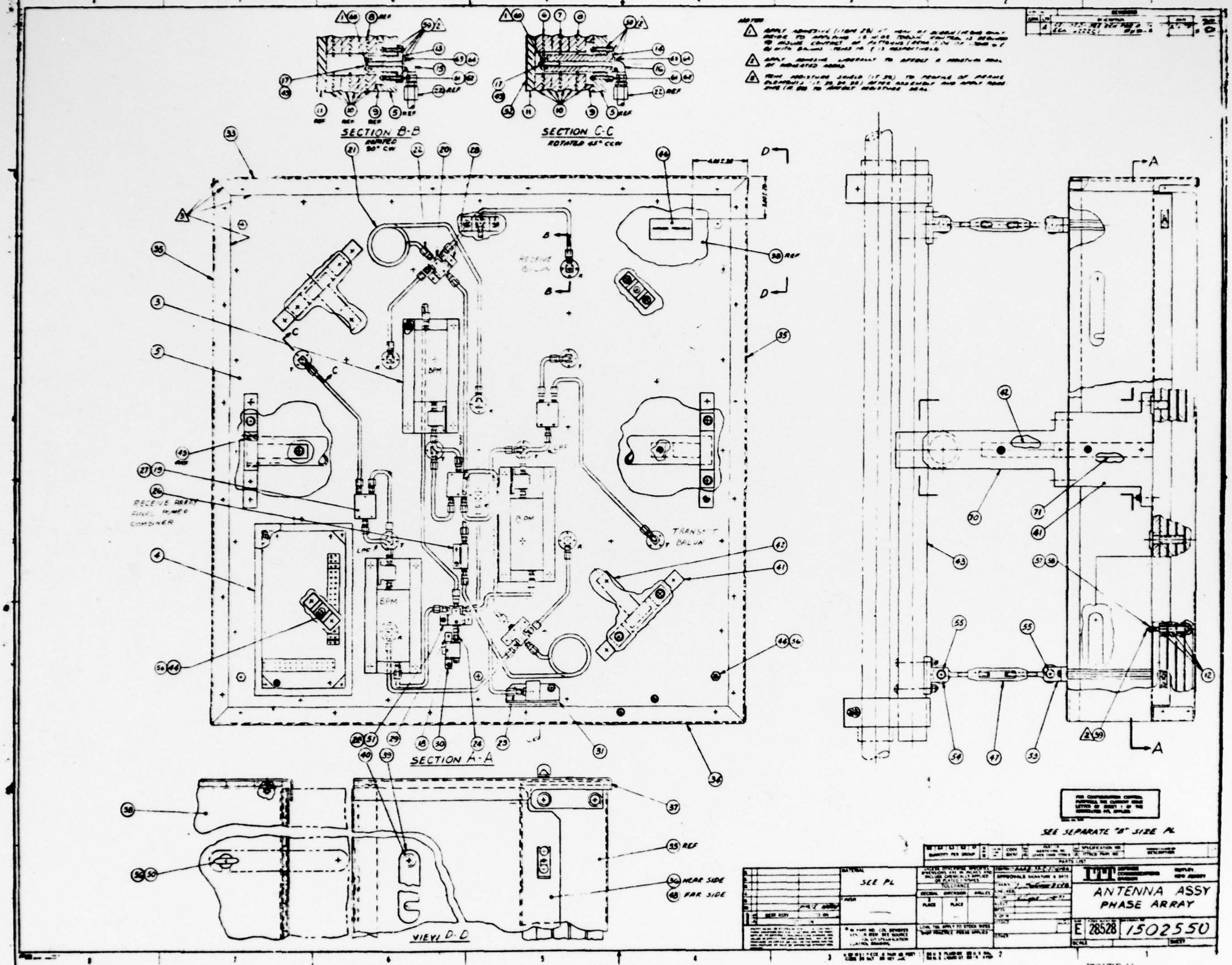

SECTION B-B
ROTATED 90° CW
SECTION C-C
ROTATED 45° CCW
RECEIVE BALUN
TRANSMIT BALUN
BPM
RECEIVE ARRAY FINAL POWER COMBINER
SECTION A-A
VIEW D-D
NEAR SIDE
FAR SIDE
SEE SEPARATE "B" SIZE PL
SEE PL
ANTENNA ASSY
PHASE ARRAY
E 28528 1502550

FIGURE 11

DWG NO. PL1502550

REVISIONS

— ORIGINAL ISSUE

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	SH 1 - REV ASSY & PL SH INDEX SH 3 - CHAGED ITEM 41, 42 & 43 QTY, ADDED ITEMS 70 & 71 ECN1G222C1	3/5/79	

ASSEMBLY SHEET/ ISSUE INDEX					
SHEET NO.	1	2	3	4	5
ISSUE LTR.	A				

SHEET NO	1	2	3	4	5
ISSUE LTR	A	-	A		

* IN PART NO. COL DENOTES VENDOR ITEM: SEE SOURCE CONTROL OR SPECIFICATION CONTROL DRAWING.

G5	G4	G3	G2	G1	U OF M	ITEM OR FIND NO.	CODE IDENT	SIZE	PART OR IDENTIFYING NO. OTHER THAN ITTDCD	SIZE	SPECIFICATION NO. ITTDCD PART NO.	NOMENCLATURE OR DESCRIPTION	ITTDCD SOURCE
QUANTITY PER GROUP													

PARTS LIST

GROUP	SIZE	NEXT ASSY	USED ON
G			
G			
G			
G			
G			
G1			PHASE ARRAY

APPLICATION

MATERIAL —

FINISH —

COML TOL APPLY TO STK SIZES

SHOP PRACTICE. P9938 APPLIES

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES

TOLERANCE

DECIMAL DIMENSION		ANGLES
2 PLACE	3 PLACE	
—	—	

CONTR DAAB-07-C-77-0146
DWN 10/17/78
CKD
APPD 1-11-79
ITTDCD

ITT DEFENSE COMMUNICATIONS DIVISION NUTLEY, NEW JERSEY

ANTENNA ASSY, PHASE ARRAY

SIZE	CODE IDENT NO.	DRAWING NO.
B	28528	PL1502550

SCALE NONE SHEET 1 OF 3

U OF M CODE | 1 PIECE 5 SET 6 PAIR 20 REF DOC 32 FEET 52 U. S. FLUID OZ 54 U. S. LIQUID QT. 55 U. S. GAL. 68 LB., AVDP.

ITTDCD D5222 (B)-V REV. 3/73

E7115 188 3/74

PARTS LIST	ITT DEFENSE COMMUNICATIONS DIVISION, NUTLEY, NEW JERSEY	CONTRACT NO.	DWG SIZE B	CODE 28528	DRAWING NUMBER PL1502550	REV LTR -

SEE COVER SHEET FOR LIST TITLE, REVISION AND AUTHENTICATION	U OF M CODE: 1 PIECE, 5 SET, 6 PAIR, 20 REF DOC, 32 FEET, 52 U.S. FLUID OZ, 54 U.S. LIQUID QT, 55 U.S. GAL, 68 LB AVDP	* IN PART NO. COL. DENOTES VENDOR ITEM. SEE SOURCE OR SPECIFICATION CONTROL DWG.	SHT 2

QUANTITY PER GROUP G3	G2	G1	U OF M	ITEM/FIND NO	CODE IDENT	PART OR IDENTIFYING NO. OTHER THAN ITTDCD	SIZE	SPECIFICATION NO. ITTDCD PART NO.	NOMENCLATURE OR DESCRIPTION	ITTDCD SOURCE
		REF	20	1			E	1502550	ANTENNA ASSY, PHASED ARRAY	
		REF	20	2			B	1502585G1	BLOCK DIAG	
		3	1	3			D	1502557G1	BASIC POWER MODULE ASSY (A1, A2, A3)	
		1	1	4			A	PL1502560G1	ANTENNA, DC POWER DISTRIBUTION/BITE BOX	
		1	1	5			E	1502569G1	PLATE, GROUND PLANE (HEXCEL)	
		1	1	6				1502579G1	MASTER DRAWING (TRANSMITTER)	
		1	1	7				1502580G1	MASTER DRAWING (POLARIZER)	
		1	1	8				1502581G1	MASTER DRAWING (RECEIVER)	
		1	1	9			D	1502570G1	INSULATOR	
		6	1	10			D	1502570G2	INSULATOR	
		1		11			D	1502570G3	INSULATOR	
		99	1	12			B	1502561G1	SPACER, INSULATOR	
		6	1	13			B	1502562G2	HOUSING, BALUN, (RCVR)	
		6	1	14			B	1502562G1	HOUSING, BALUN, (XMTR)	
		6	1	15			B	1502563G2	CONNECTOR, MODIFIED, BALUN (RCVR)	
		6	1	16			B	1502563G1	CONNECTOR, MODIFIED, BALUN (XMTR)	
		12	1	17			B	1502606G1	NUT, BALUN - NO. 2-56	
		1	1	18	4M959	3CI63			ISOLATOR (JUNCTION DEVICES)	
		4	1	19	12457	PDM-20-4.7G			SPLITTER, 2 WAY	
		3	1	20			B	1502582G1	SPLITTER, 3 WAY ARTWORK	
		AR	32	21		RG-401/U		MIL-C-17/129	CABLE, RF, COAXIAL, .250 DIA SEMIRIGID, 50 OHM	
		41	1	22	16179	OSM 201-5			PLUG, .250 IN., SOLID DIELECTRIC, SEMI-RIGID CABLE	
		1	1	23	16179	OSM 202-5			JACK, .250 IN., SOLID DIELECTRIC, SEMI-RIGID CABLE	
		1	1	24	16179	OSM 218			ADAPTER, STRAIGHT PLUG/PLUG	
		AR	52	25				MIL-S-22473	SEALING ADHESIVE (BLUE) GRADE CV. (LOCKTITE)	
		1	1	26			B	1502566G1	BRACKET, SPLITER, 2 WAY	
		3	1	27			B	1502567G1	SPACER, SPLITER, 2 WAY	
		3	1	28			B	1502565G1	BRACKET, SPLITER, 3 WAY	
		1	1	29			B	1502564 G1	ANGLE, ISOLATOR	
		1	1	30			B	1502564 G2	ANGLE, ISOLATOR	
		1	1	31			C	1502555G1	WAVEGUIDE ADAPTER ASSY	
		1	1	32			B	1502583G1	SHIELD, MOISTURE	

6711 ISS 3/74

PARTS LIST	ITT DEFENSE COMMUNICATIONS DIVISION, NUTLEY, NEW JERSEY	CONTRACT NO.	DWG SIZE B	CODE 28528	DRAWING NUMBER PL 1502550	REV LTR A

SEE COVER SHEET FOR LIST TITLE, REVISION AND AUTHENTICATION	U OF M CODE: 1 PIECE, 5 SET, 6 PAIR, 20 REF DOC, 32 FEET, 52 U.S. FLUID OZ, 54 U.S. LIQUID QT., 55 U.S. GAL, 68 LB AVDP	* IN PART NO. COL. DENOTES VENDOR ITEM: SEE SOURCE OR SPECIFICATION CONTROL DWG.	SHT 3

QUANTITY PER GROUP G3	G2	G1	U OF M	ITEM/FIND NO	CODE IDENT	PART OR IDENTIFYING NO. OTHER THAN ITTDCD	SIZE	SPECIFICATION NO. / ITTDCD PART NO.	NOMENCLATURE OR DESCRIPTION	ITTDCD SOURCE
		1	1	33			C	1502543G1	FRAME (TOP)	
		1	1	34			C	1502543G2	FRAME (BOT)	
		2	1	35			C	1502544G1	FRAME (LT & RT SIDE)	
		1	1	36			C	1502545G1	SHIELD, RAIN (RT SIDE)	
		1	1	37			C	1502546G1	SHIELD, RAIN (TOP)	
		1	1	38			D	1502547G1	SHIELD, SOLAR	
		6	1	39			B	1502548G1	ARM, LATCHING	
		6	1	40			B	1502549G1	SPACER, PIVOT (ARM)	
		4	1	41			C	1502551G1	MOUNT, ANTENNA (LOWER)	
		2	1	42			C	1502552G1	GUSSET, ANTENNA (UPPER)	
		1	1	43			C	1502553G1	ANTENNA MOUNT	
		8	1	44			B	1502554G1	POST, SOLAR SHIELD	
		1	1	46			B	1502577G1	PLATE, IDENTIFICATION	
		2	1	47					TURNBUCKLE, 3/8	
									(TURNBUCKLE INC)	
		1	1	48			C	1502545G1	SHIELD, RAIN (LT SIDE)	
		12	1	49	29440	ST-1			WASHER, BELLEVILLE (CRES)	
		6	1	50			B	1133402G1	THUMBSCREW	
		1	1	51			B	1502568G1	SPACER, SPLITER, 3 WAY	
				52						
		4	1	53			D	1502574G1	SUPPORT, TURNBUCKLE	
		2	1	54			D	1502575G1	SUPPORT, TURNBUCKLE	
		4	1	55			B	1502576G1	SPACER, PIVOT (TURNBUCKLE)	
		AR	1	56		MS15795-806		FF-W-92	WASHER, FLAT, NO. 10	
		33	1	57					ROD, NYLON, NO. 10-32x3.5 LG	
		66	1	58					NUT, NYLON, NO. 10-32	
		AR	52	59			B	1133290G1	ADHESIVE, SEALANT	
									(GE RTV 3140)	
		48	1	60		MS51957		FF-S-92	SCREW, MACH, PN HD	
									0-80 x .25 LG.	
		48	1	61				FF-S-92	SCREW, MACH, PN HD	
									4-40 x .75 LG.	
		48	1	62				FF-W-84	WASHER, SPLIT LOCK #4	
		48	1	63				FF-S-92	SCREW, MACH, PN HD	
									2-56 x .25 LG	
		48	1	64				FF-W-84	WASHER, SPLIT LOCK #2	
		19	1	65				FF-S-92	SCREW, MACH. PN HD	
									6-32 x .38 LG	
		48	1	66				FF-S-92	SCREW, MACH PN HD	
									10-32 x .38 LG	
		48	1	67		MS15795-810		FF-W-92	WASHER, FLAT, NO. 10	
				68					TAPE, TEFLON	
				69			A	1502595G1	3 WAY POWER DIVIDER	
									HOUSING	
		2	1	70			C	1502614G1	MOUNT, ANTENNA (UPPER)	
		4	1	71			C	1502615G1	GUSSET, ANTENNA (LOWER)	

23

Above the ground plane structure is a solar shield (item 38). This aluminum plate is painted with a solar reflecting paint. The side and top doors are hinged to this shield. The shield is mounted to the honeycomb ground plane by 8 metal standoffs. This solar shield is not a structural member.

Items 42 and 70 provide a stiff interface from the antenna assembly through the solar shield to the positioner (Item 43). The positioner clamps to a corner member of the AB-216 tower. Vertical positioning is accomplished by rotating the two turnbuckles (item 47) while horizontal positioning is accomplished by rotating the positioner about the tower corner member.

IPA RF power is applied from the control cabinet to Item 18, isolator. The isolator output fees Item 20, three way power divider. This divider feeds each BPM via semirigid coax cable. The BPM output goes through an isolator to a coax cable type low pass filter, both the isolator and the low pass filter are part of the BPM assembly. The LPF feeds - item 19 - a 2 way power divider. The outputs of the power divider feeds two transmit baluns (T).

For the receive array, the 6 receive baluns (R) feed 2 three way power dividers - (Item 20): which act as combiners for the receive array. The output of the 3-way dividers (combiners) are combined in a 2 way power combiner. The output of the 2 way power combiner is fed to a Coax to Waveguide transition, (Part of Item 31) providing the waveguide interface (WR-187) to the AN/GRC-143 Receiver. This final power combiner is mounted on edge.

The DC power distribution box (Item 4) receives the DC power from the control cabinet and distributes power to the three basic power modules. (DC cabling not shown on the assembly drawing). This box also accepts the RF power detector signal from each BPM and sends these signals to the control cabinet for Front Panel Meter display.

II F 1.B TRADE OFF ANALYSES

SINGLE VS. DUAL LAYER ANTENNA SELECTION

One trade off considered early in the program was to determine the best approach for the antenna design. Two possibilities exist. The first choice involves a plane antenna with both the receive and transmit dipoles printed on one laminate. The second choice involves separate dipole laminates for each antenna with an intervening polarizer laminate. The following discussion considers the alternatives.

Statement of Conclusions

The choice of single versus dual layered antenna configuration must weigh the immediate needs of this R & D program against the long-term needs of future production programs. Viewed in terms of program goals, the dual layer antenna is the logical choice for developing a one-tenth size antenna-amplifier that demonstrates the feasibility for space-addition of low power modules for solid-state troposcatter amplifier systems. Conversely, the single layer structure is the logical choice for a field serviceable antenna system due to lower weight and cost plus ease of maintenance.

Technical Description

The antenna is required to be dual polarized: two independent arrays superimposed in a single aperture, independent access and distribution networks, efficient radiation of two uncoupled pencil beams of orthogonal polarizations. Two alternatives for the practical realization of a dual antenna system using printed circuit techniques are:

a) Single layer - a single (thin) printed circuit sheet containing two dipole arrays with their associated distribution circuits (corporate feeds), positioned above a single ground plane. The risk feature of this structure is the attainment of a printed layout which accommodates two orthogonal array-feed systems with a minimum of cross coupling.

b) Dual layer - a structure in cross-section of three (thin) printed circuit sheets positioned above a ground plane, and superimposed one above the other. Two sheets each contain one printed planar dipole array with corporate feed; the third sheet contains a printed "polarized" ground plane, i.e., transparent to one polarization and totally reflecting to the orthogonal polarization. The difficult aspect of this structure is the three dimensional interlacing of two independent (dual) antenna systems with a minimum of cross coupling.

In the development of the 1:10 scale antenna, the dual layer design provides a known basis of antenna performance on which to build an integrated amplifier system. That basis is the expertise acquired by ITT in developing similar antenna configurations at X-band. Performance consistent with the needs of this program were attained at X-band.

Opposing this advantage are the potential benefits of the single layer antenna: improved electrical performance, improved mechanical features, reduced complexity for manufacture and assembly, and reduced cost.

Applied to the 1:10 model, the single layer design if optimally completed will result in only marginally improved electrical performance; estimate: 0.5 to 1 dB gain, 1 to 2 dB lower near-in sidelobes, 2 to 5 dB lower spurious sidelobes, 2 to 5 dB improved polarization isolation, and a small VSWR improvement. Mechanically, the 1:10 model antenna would be 20 lbs. lighter and 4 inches thinner. On a feasibility demonstration of a concept, as is here, the efforts expended on construction complexity, assembly, and material cost are not a significant part of the total and are not, properly, goals: hence they are minor tradeoff factors.

The single layer advantages, in sum, add little to the goals of the 1:10 model that cannot be retrieved at any stage of follow-on programs. The single layer antenna adds no conceptual change to the system and is viewed as a "component"

improvement, much as a new transistor. The value of these components must be continually reviewed against the program goals: feasibility demonstration, costs, produceability, etc. Consequently, it is concluded that the dual layer antenna is the better choice for the feasibility phase of this program because it adequately fills its functional roles for space-addition of power with minimum risk of non-performance. The single layer design, though very attractive for field use, would load down a feasibility task with a major effort whose results run the risk of severly under-achieving at worse, and at best marginally improving the dual layer capability.

1-PIECE VS. SECTIONALIZED CONSTRUCTION-VENDOR SURVEY

Another investigation early in the program was the consideration of fabricating single large array sheets (38" x 38") or sectionalizing to smaller sheets (2, 3, 4, etc.) to form the large single array. Manufacturers with capabilities to supply and process large laminates had to be located. This was accomplished. The 3M Corporation & Keene, Inc., supply teflon impregnated Fiberglass and Chempar Corp., Penn. processes large laminate sheets.

The single large board approach has certain obvious advantages such as decreased handling, simpler alignment procedures, and electrical continuity.

A sectionalized, piece-part approach would serve to compound problems such as continuity, tolerance/registration, and system integrity.

Several prospective array material were investigated and evaluated during the initial survey. A comparison of materials and significant properties is shown in Table I. Based upon available material size, dielectric constant and loss tangent, the Keene material was chosen.

As a result of this survey, the single piece approach for each antenna has been selected.

MATERIAL AND MANUFACTURER

Property	K-6098 LX **Teflon/Glass Cloth Laminate** 3-M Corp. 155 Fourth Ave. Needham Heights, MA 02194 *Keene Corp Chase Foster Division P.O. Box 700 Newark, Delaware 19711	RT Duroid 5880 Glass Micro Fiber Reinforced Teflon Rogers Corp. Chandler, Arizona 85224	Polybuta Diene (Reinforced with fiberglass "E" Glass) Brunswick Corp.	Polybuta Diene (Reinforced with fiberglass) Quartz Glass Brunswick Corp.	Tellite (Irradiated Polyolefin) Tellite Corp.	Z-Tron Polyphenylene Oxide Po ymer Corp.
Electrical						
Dielectric Constant (K) at 10-GHz	2.45 ± .04 (at X-band)	2.20 ± .03 (at 10GHz)	3.6 ± .2 (35% Resin/Glass)	2.8 ± .2 (35% Resin/Glass)	2.32 (at 4.3 GHz)	2.55 ± .02 (at 8.5GHz)
Dissipation Factor (DF) at 10-GHz	.0018	.0009	.008 (")	.003 (")	.00015	.0015
Physical						
Coefficient of Thermal Expansion						
Lengthwise and crosswise	9 to 10 x 10^{-6} per °C	32 to 67 x 10^{-6} per °C	2.25 x 10^{-6} per °F	2.25 x 10^{-6} per °F		
Thickness	120 to 130 x 10^{-6} per °C	160 to 200 x 10^{-6} per °C				
Thermal Conductivity	2.6 x 10^{-4} Cal/Sec °C Cm	6.25 x 10^{-4} cal/sec °C Cm	0.7 to 1.7 BTU-IN/ft^2 °F (at 800°F)	0.7 to 1.7 $\frac{\text{BTU-IN}}{\text{FT}^2\ \text{°F}}$ (at 800°F)		
Specific Gravity (Unclad)	2.2	2.18				
Water Absorption	0.024%	0.02%				
Mechanical						
Flexural Strength						
Lengthwise	16,500 Psi	5,000				
Crosswise	13,500 Psi	4,400				
Young's Modulus (Tensile) (E)	0.7 x 10^6 Psi	0.2 x 10^6 Psi				
Manufacturing						
Thickness Tolerance	±.002 inch	±.002 inch	±.003 inch	±.003 inch		
Shrinkage After Etching	0.2 Mils/inch					
Available Sizes	36" x 36" Keene 38" x 48" *Selected as the vendor for this program	16" x 40" STD. (could possibly "seam match" sheets up to 32" x 36" with some property differences)	36" x 36"	36" x 36"	22 1/2" x 32" STD	16" x 24" STD

TABLE I

II F 2. ANTENNA ELECTRICAL DESIGN

The electrical design of the antenna required several steps before a final configuration was chosen. These steps included:

- Analyses of previous printed antenna performance and extending this design to 4.4 - 5.0 GHz band.
- Computer Aid Design to aid the selection of antenna taper.
- Development of the balun (unbalanced to balance impedance transformer) to couple amplifier power to the antenna dipole structure.
- Evaluation of various laminates to select the best type.
- Development of power dividers which maintain impedance integrity to minimize impact on Balun VSWR.

PRIOR MAT-STRIP EXPERIENCE

Previous experience at ITT in Mat-Strip techniques has been at the SHF SATCOM communications band. Two efforts were completed:

- A 4 module array with a rear waveguide feed system providing dual circular polarizations, uniform illumination, and 2 axis monopulse tracking capability; the aperture size was 2.5 x 2.5 ft.
- A single array aperture of 18 inch diameter provided dual circular polarization; the printed array incorporated an unequal way power divider which provided a tapered illumination for sidelobe reduction.

In the initial Mat-Strip development, spurious sidelobe were observed which were traced to radiation of reflected waves in the corporate feed. A design change in the corporate feed physical layout eliminated the spurious lobe completely at band center and partially at band edges. This program's attempt to scale the design change to C-Band was off by several hundred MHz so that spurious lobes occur at the high end of the band. This results in a loss of gain. A detailed analysis of the spurious lobe angle in space versus frequency, and the geometry of the corporate feed shows the radiation is a grating lobe of radiating elements of twice the dipole spacing. This spacing corresponds to the location of the set of 4 way dividers immediately feeding sets of 2 x 2 dipole sub-arrays. Thus it is implied that dipole reflections produce standing waves at the nearest feed line junctions which radiate as a coherent array. Further artwork interations to reduce these lobes could consist of:

- Optimize dipole - divider spacing to center response
- Randomize divider locations to defocus sidelobe
- Decrease dipole spacing to move sidelobe into cutoff- non visible space
- Add resistive element at divider to suppress spurious current.

The estimate expected spurious lobes would be, respectively: $>$25 dB, $>$30 dB $>$ 30 dB, $>$40 dB.

Mat-Strip Corporate Feed Development

The dipole array is excited by a corporate feed which is realized partially in Mat-Strip, to combine a sub-array of dipoles into a single port, and partially as a coaxial structure external to the antenna to combine sub-arrays. To attain the Mat-Strip corporate feed, two basic building blocks were required to be designed: a Mat-Strip 2 equal-way divider, and a Mat-Strip to coax Balun transformer.

The printed circuit power divider was developed as a "T" junction with impedance transformers in all 3 legs at the junction. This was a realization of a two section Tchebyschev transformer of 1.05:1 maximum VSWR. Using Computer Aided Design, line widths corresponding to the required impedance levels of the transformers were used in the printed circuit development. Minor trimming was required because of junction effects, and final tests showed VSWR's well under 1.05:1 across the band. Since all tapering is done external to the Mat-Strip, the required corporate feed for each sub-array can be realized by using a multiplicity of the one type binary power divider. This requires that the untapered sub-array be square and of 2^N dipoles; 2^4 or 4 x 4 dipoles were used as the basic building blocks, final integration of the full array required non-binary dividers. The binary type corporate feed results in equi-phase and amplitude excitation of the sub-array. The possible build-up of VSWR due to successive power divisions was checked experimentally by comparing VSWR's of the dipoles fed directly from a balun to that of a 4 x 4 dipole array with its corporate feed composed of binary dividers; no appreciable differences were noted indicating the individual dividers are virtually transparent.

The balun development consisted of two parts. First, optimization of the geometry of the printed circuitry which interfaces with a coaxial line such that a transformation from the grounded coax to the ungrounded parallel wire Mat-Strip is effected with a minimum of radiation loss. This was accomplished by a division of the junction into two Mat-Strip lines of $100\,\Omega$ each, an equal power division and match to $50\,\Omega$ coax, and a tapering of the lower conductors adjacent to the coaxial ground

as is done in the "infinite balun". Second, an impedance transformer was designed into the coaxial line immediately adjacent to the Mat-Strip junction to match the junction effects. The transformer was experimentally optmized and overall balun performance of 1.15:1 maximum VSWR and 0.5 dB maximum loss were attained over the band.

Because of the lack of standardized test equipment in the parallel wire line of the Mat-Strip media, all development was done with a duplication of the circuitry in a back-to-back configuration. Thus, two baluns were tested with their Mat-Strip lines mated and various interconnecting lengths were used to account for phasing effects. Simiarly, the power divider development utilized back-to-back power dividers fed at each end by baluns and the results compared to the previous dual balun results to determined the VSWR contributed by the power dividers.

Radome and Filler Material

The radome and filler (inter-layer support) material is a closed cell foam of very low loss and dielectric constant; the material is Ecco-foam type PP-2#/CF from Emerson-Cumming, Inc., Canton, Massachusetts. The material chosen provides the necessary mechanical support with satisfactory environmental properties of very low water absorption and wide temperature range. The electrical effects are of two types: transmission characteristics as a circuit element, and error effects due to material variation.

Transmission consists of the error free performance as part of the material in the antenna structure; this is completely analogus to a transmission line containing a dielectric support "slug", or as here a composite of dieletric slugs. The effect of the slug is to change the impedance, phase shift and attenuation. The impedance and phase are accounted for in the development of the dipole matching with all layers in place; it is the effect of attenuation that must be determined. This requires considering the Mat-Strip PCB's as well as the foam, in their actual circuit configuration, i.e., as backed by a totally reflecting ground plane which produces a "resonant" or standing wave field. The free space attenuation of a dielectric material is

$$\alpha_{-dB} = \frac{27.3 \sqrt{E} \tan\delta}{\lambda_o} \times L$$

where L = length

λ_o = free space wavelength $\approx$ 11.8/F - GHz, inches

E = material dielectric constant

Tan δ = material loss tangent.

Thus, for a structure consisting of 3 PCB's (Printed Circuit Boards) of Teflon-fiberglass material .062 inches thick each, and 4 foam layers (3 inter-layers plus a radome) totaling 2.5 inches, the loss at 5 GHz is:

$$\alpha_d = \alpha_{PCB} + \alpha_{FOAM} = \frac{27.3}{11.8/5} \left\{ (.187) \sqrt{E_{PCB}} \tan\delta_{PCB} + (2.5) \sqrt{E_f} \tan\delta_f \right\}$$

for $E_{PCB} = 2.45$, $\tan\delta_{PCB} = .0018$

$E_f = 1.04$, $\tan\delta_f = .0008$

then $\alpha_d = .0326 + .0224 = .0550$ dB

Finally, the "resonant" effect is approximated by a factor of 4 in dB which results from an effective increase in path length due to reflection, thus

$$\alpha_T = 4 \times .055 = .22 \text{ dB}$$

The variation in material across a large aperture may be significant in percent for the foam material, however, a large percent of a small quantity remains a small quantity. Thus, a 100% variation in dielectric constant, for example, from 1.04 to 1.08 would increase the loss of .0224 dB to .0228 dB: an insignificant amount. Similarly, the PCB material will have insignificant effect on the **space** wave both for the above reason and the closer control of manufacturing tolerance. Therefore, it is concluded no significant error effects are inherent in the filler and radome configuration.

Receiver Array Design

The receive array is identical to the transmit array except in polarization (-45° off Horizontal). The polarization will be attained by 90° rotation of dipoles in the array. Another main difference is the positioning of the receive array behind the transmit array in the aperture. This requires that the received signal is propagated thru the transmit array, polarizer layer and filler material. The affect of this is to reduce the overall receiver array gain.

CAD ARRAY PROGRAMS (COMPUTER AIDED DESIGN)

Introduction: Two type programs have been written to apply CAD in the antenna development.

Program I - Calculates and plots relative far field amplitude in dB versus angular position, usually scan angle (Θ) with the second coordinate angle (ϕ) held constant. Fine incrementing of the angle and interconnection of points in plotting, provide a continuous curve; a point by point tabulation can be an alternative output. Since this type pattern is a cross-section of the volume of space into which the antenna radiates, many patterns are required to determine the full spatial response. Characteristically, principle planes of conern are identified and plotted according to the antenna type and system application; thus, an assumption or pre-knowledge is needed to select the pattern coordinates to be plotted. The program incorporates the following:

- Dipole element pattern - represented by an analytic equation derived for sinusoidal excitation.
- Ground plane pattern - represented by an image dipole array.
- Array factor - calculated by vectorial summation of all dipole elements.
- Illumination - amplitude and phase of current at each dipole can be specified and applied in the vector sum; this includes error functions of which the random type can be generated by the program.

Figure 12 shows plots generated by Program I.

Program II - Calculates and plots a three dimensional far field pattern of amplitude versus both angular coordinates and, also calculates antenna directivity, an aspect of gain. The 3-D pattern plot is analogous to a topological or contour map which represents elevation at a location specified by longitude and latitude; here, field amplitude is plotted versus spatial position and where the plane of the map represents the surface of the far-field hemi-sphere- the surface of constant distance from the antenna center. The computer output to a teletype terminal is

used for this plot by equating the two orthogonal spatial coordinates (Sin Θ COS ϕ, COS Θ SIN ϕ) with row-column locations, and the amplitude with an alpha-numeric symbol suitably defined in a key-code table. Thus, this program output surveys the full extent of the radiated space at a selectable number of discreet points; a feature which compliments Program I by provid g the "pre-knowledge" for choosing a particular cross-section to be plotted in the amplitude versus scan angle format. Program II, in addition, calculates directivity as the ratio of boresight power to the sum of the power at all points averaged over the full surface; the directivity output is printed as a number in dB following the pattern plot. The program features:

- Calculation of the dipole element pattern by direct integration of the (sinusoidal) current along the dipole length. This allows direct use of the program for harmonic analysis as well as fundamental analysis over any bandwidth.
- Calculation of ground plane effect by image dipole array at twice the ground plane spacing; again this provides extended bandwidth and harmonic analysis capability.
- Calculation of array, or lattice, factor by vectorial summation of all array elements at any far field point in space thereby providing a non-approximate base for analyzing any shape array, or grid; or error pattern.
- Provision for specification of any amplitude and phase excitation in the dipole array; this includes generation of random excitations.
- Calculation of directivity, or gain.
- Variable incrementing of the coordinate space angles for finer steps at a broadside main beam angles. This is accomplished by a projection of the surface area of the hemi-sphere on a plane parallel to the array plane (common normal), and variably stepping the scan angle (Θ). This provides program efficiency and a systematic method to determine accuracy because resolution and error asymptotically approach zero as the number of increments is increased.

Program II Output Format

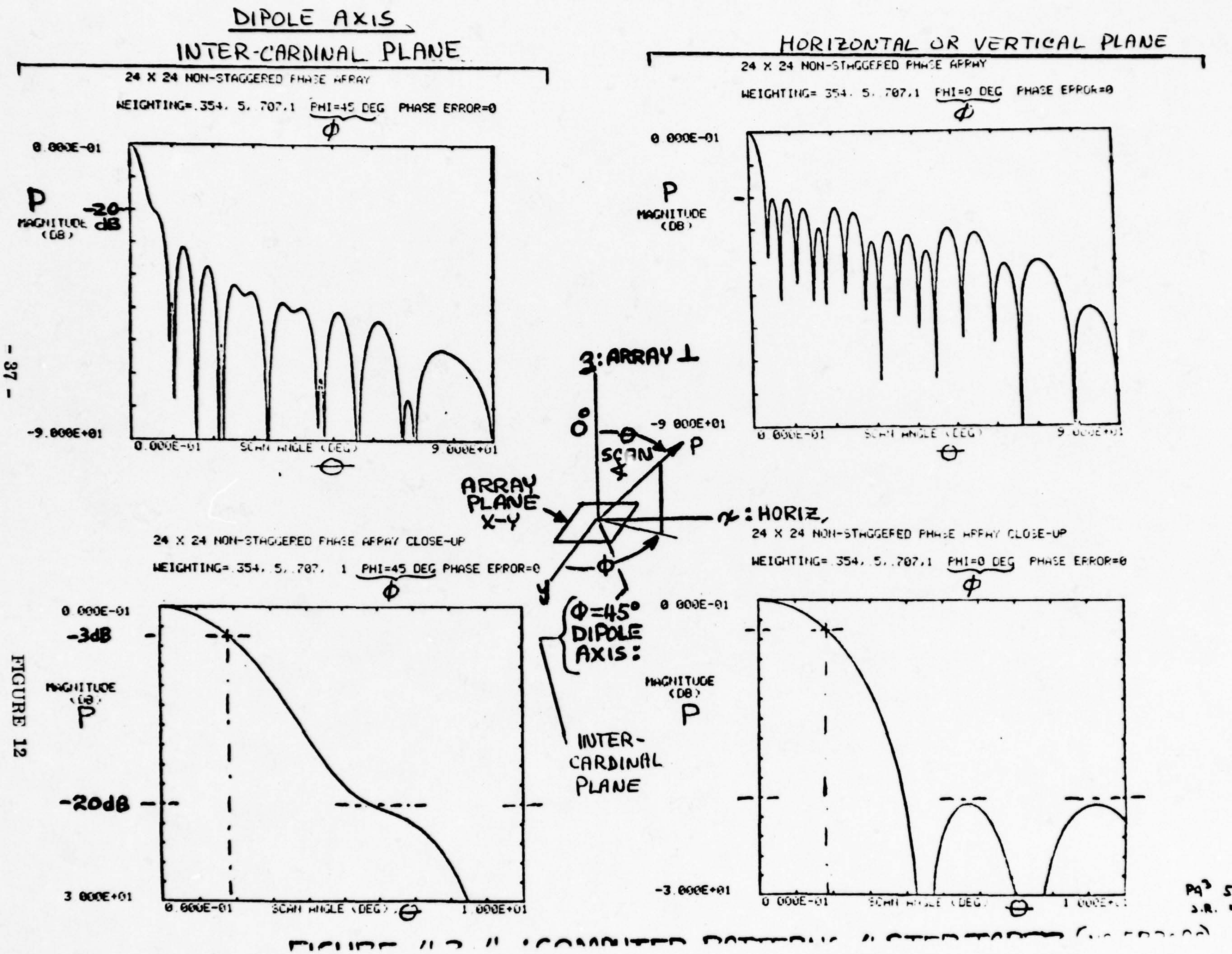
The contour map produced by this program is shown in Figure 13. Displayed is a series of typed alpha-numeric symbols which have the following meanings:

- Value of the symbol is assigned, arbitrarily, to a range of powers calculated by the program in dB. Each program run establishes a table of symbol versus power; all positive dB are loss ratios.
- Location of a symbol in the printed array corresponds to a unique pair of coordinate angles: θ, ϕ. The coordinate pair is systematically stepped over a full hemi-sphere using the following angular ranges: $0 \leq \theta \leq 90^{\circ}$, $0^{\circ} \leq \phi \leq 360^{\circ}$. In cases of known symmetry a lesser range is used. Note that the outer perimeter contour is a circular projection of the hemi-sphere on a plane which degenerates here to an ellipse due to the unequal width versus height inherent in a typing format; there are, however, an equal number of vertical and horizontal characters on each major axis.
- Gain is outputed as a single numeric, in dB, referenced to the angular position: $\phi = 0^{\circ}$; $\theta = 0^{\circ}$. This is the axis normal to the array and the nominal center of the main pencil beam. Thus, the gain reflects losses due to beam squint as well as due to beamwidth and sidelobe structure. The dB output is a positive number for the increase in power of the array compared to a single isotropic radiator of zero dB power.

Thus, the data format shows the usual pattern characteristics of amplitude versus coordinate scan angles. Beam peaks, nulls, sidelobes can be located by "reading" their amplitudes from the Key-code table; beam location, beamwidth, sidelobe or null location can be read by counting their grid position and de-incrementing according to the projection scheme.

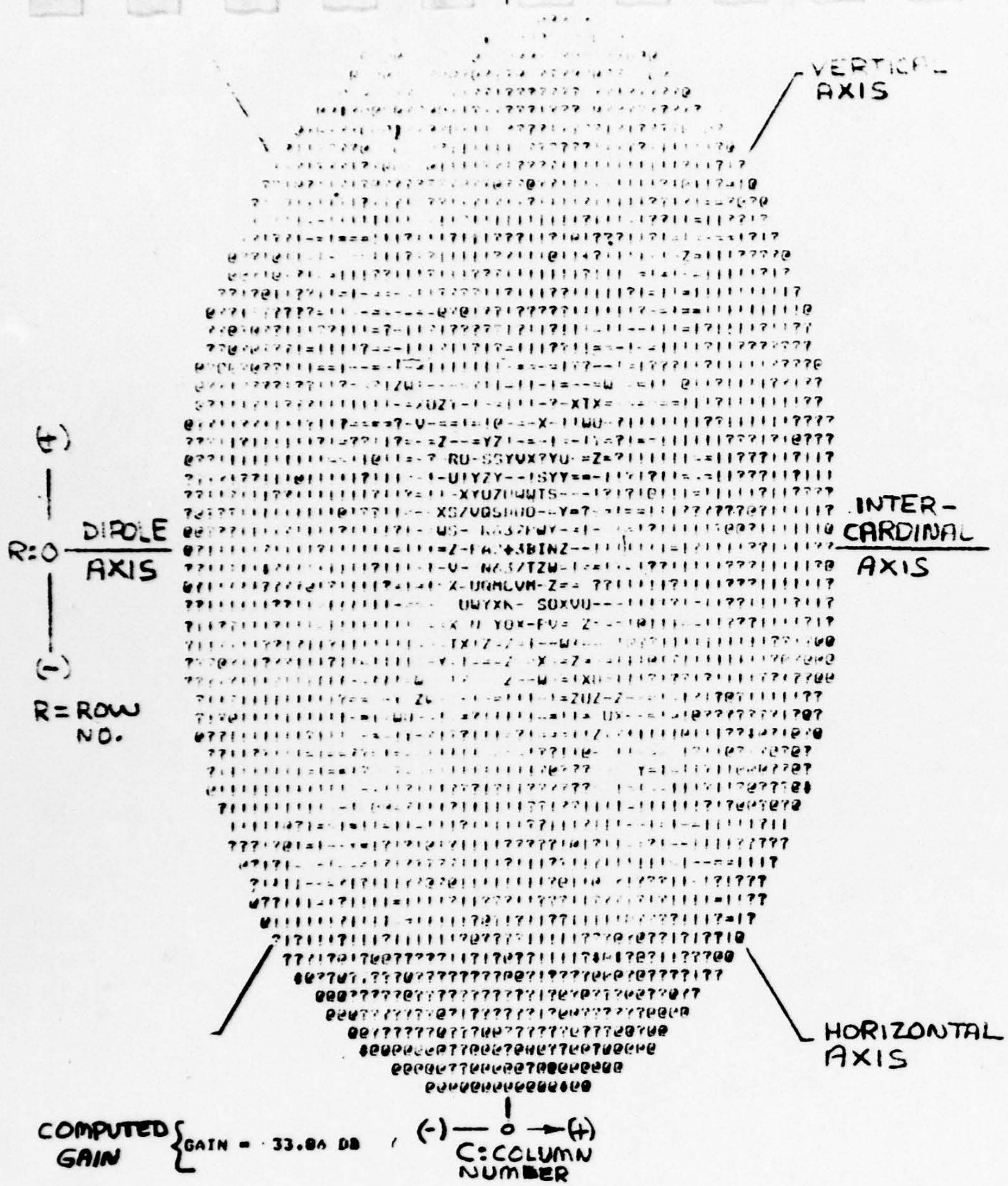
Program Validation

Both programs were validated by applying cases of known solution: uniform illumination of a square array which has a well known analytic solution; multiple



DIPOLE AXIS
INTER-CARDINAL PLANE
24 X 24 NON-STAGGERED PHASE ARRAY
WEIGHTING=.354, 5, 707,1 PHI=45 DEG PHASE ERROR=0
0.000E-01
-20 dB
P
MAGNITUDE (DB)
-9.000E+01
0.000E-01
SCAN ANGLE (DEG)
9.000E+01
HORIZONTAL OR VERTICAL PLANE
24 X 24 NON-STAGGERED PHASE ARRAY
WEIGHTING= 354, 5, 707,1 PHI=0 DEG PHASE ERROR=0
0.000E-01
-9.000E+01
3: ARRAY ⊥
SCAN
ARRAY PLANE X-Y
x: HORIZ,
Φ=45° DIPOLE AXIS:
INTER-CARDINAL PLANE
24 X 24 NON-STAGGERED PHASE ARRAY CLOSE-UP
WEIGHTING=.354, 5, 707, 1 PHI=45 DEG PHASE ERROR=0
-3dB
-20dB
3.000E+01
1.000E+01
WEIGHTING=.354, 5, 707,1 PHI=0 DEG PHASE ERROR=0
-3.000E+01

FIGURE 12



[illegible] = 1.500 IN.

[illegible]

[illegible] 0.[illegible] WAVELENGTHS AT 4.2 G[illegible]

[illegible] [illegible].500 WAVELENGTHS AT [illegible]

[illegible]

* ANGLE INCREMENT AT CENTER = 1.910 DEG.

[illegible] ERROR (UNIFORM DISTR.) = 20.00 DEG.
[illegible] AMPLITUDE ERROR (GAUSSIAN DISTR.) = 1.50 DB
3 SIGMA ELEMENT PHASE ERROR (GAUSSIAN DISTR.) = 20.00 DEG.
3 SIGMA ELEMENT AMPLITUDE ERROR (GAUSSIAN DISTR.) = 0.30 DB

VOLTAGE WEIGHTING FACTORS FOR GROUPS OF 4 DIPOLES

0.500	0.500	0.354	0.354	0.354	0.354	0.354	0.354	0.354	0.354	0.500	0.500
0.500	0.500	0.354	0.354	0.354	0.354	0.354	0.354	0.354	0.354	0.500	0.500
0.354	0.354	0.500	0.500	0.707	0.707	0.707	0.707	0.500	0.500	0.354	0.354
0.354	0.354	0.500	0.500	0.707	0.707	0.707	0.707	0.500	0.500	0.354	0.354
0.354	0.354	0.707	0.707	1.000	1.000	1.000	1.000	0.707	0.707	0.354	0.354
0.354	0.354	0.707	0.707	1.000	1.000	1.000	1.000	0.707	0.707	0.354	0.354
0.354	0.354	0.707	0.707	1.000	1.000	1.000	1.000	0.707	0.707	0.354	0.354
0.354	0.354	0.707	0.707	1.000	1.000	1.000	1.000	0.707	0.707	0.354	0.354
0.354	0.354	0.500	0.500	0.707	0.707	0.707	0.707	0.500	0.500	0.354	0.354
0.354	0.354	0.500	0.500	0.707	0.707	0.707	0.707	0.500	0.500	0.354	0.354
0.500	0.500	0.354	0.354	0.354	0.354	0.354	0.354	0.354	0.354	0.500	0.500
0.500	0.500	0.354	0.354	0.354	0.354	0.354	0.354	0.354	0.354	0.500	0.500

PLOTTING FUNCTION

POWER VS SPACE $\measuredangle s: \Theta, \Phi$

KEY TO DB VALUES OF CHARACTERS ON PLOT

```
       0 1 2 3 4 5 6 7 8 9

 -10   ::::::::::::::::::..
   0   00112233445566778899
  10   AABBCCDDEEFFGHIJKLMN
  20   OPQRSSTTUUVVWWXXYYZZ
  30   --------------------
  40   ||||||||||||||||||||
  50   ????????????????????
  60   @@@@@@@@@@@@@@@@@@@@
  70   @@@@@@@@@@@@@@@@@@@@
  80   ####################
  90   ####################
```

$\Phi = 45 + \tan^{-1}\frac{C}{R}$ DEG

$\Theta = 1.91^{*}\sqrt{C^2+R^2}$ DEG

R ≡ ROW NO. OF PLOT

C ≡ COLUMN NO. OF PLOT

* PROGRAM CALL-OUT

****** RUN NUMBER 2 ******

AMPLIFIER PHASE ERRORS (DEG.)

15.52 10.26 11.12 -16.60 17.64 -13.34 9.89 19.79 5.50 -11.28 -13.29 17.52

AMPLIFIER AMPLITUDE ERRORS (DB)

FIGURE 13

CAD-PROGRAM II CONTOUR ANTENNA PATTERN

PA[1]

beam pattern at the 2nd harmonic whose solution was hand-calculated. Both cases showed equivalent results between the program and derived solution.

Data

Details of the Antenna Performance including patterns, beamwidth, gain, ERP, and pattern degradation simulating BPM failures are included in Extend Antenna Array Tests, part of the approved test plan included in Appendix A. Included in Appendix A - Extended Antenna Array Tests - are comparisons of expected performance (as projected from Computer Aided Design) with actual performance.

IIF.3 AMPLIFIER DESIGN

During the investigation leading to an amplifier design both Silicon Bipolar and Gallium Arsenide FET (GaAsFET) transistors were evaluated. Characteristics considered most important for this system application were:

- Power Output
- Reliability
- Efficiency
- Bandwidth
- Gain
- Noise Power
- Phase Uniformity
- Cost/Watt
- Minimum Device Count
- Projections for Device Improvements in Expanding to 1 KW System

A survey of device manufacturers, including evaluation of parts, was undertaken prior to the award of this contract. The results indicated that as of June 1977:

a. Bipolar devices, developed by TRW under USA ECOM Contract DAAB07-73-C-0283 provided the greatest power output, lowest cost/watt, minimum device count and best prospects of improvements in the short term.

b. GaAsFET development, though extensive, provided low power level parts which were significantly more expensive. Higher power transistors were still limited to the development stage.

Thus the system was developed around the TRW MRA271 devices and a single cell version of this device - MRA272.

For this program, TRW felt improvements in device geometry and internal matching would improve the turn on characteristic, bandwidth and efficiency of the MRA 271/272 devices.

While these modifications were in progress, ITTDCD evaluated samples of the devices as developed for ECOM by TRW.

Bipolar Amplifier Results

The initial amplifier efforts on this program were with bipolar transistors developed by TRW Semiconductor Division for 5 GHz applications. These transistors were similar to the devices developed by TRW for the US Army Electronics Command, Fort Monmouth (ECOM) with several notable differences:

- A 5 cell power transistor design (versus 6 cell) was developed to improve yield.
- A single cell transistor was fabricated to provide a driver for the 5 cell transistor.
- Internal matching was incorporated into both transistor designs to improve bandwidth performance.

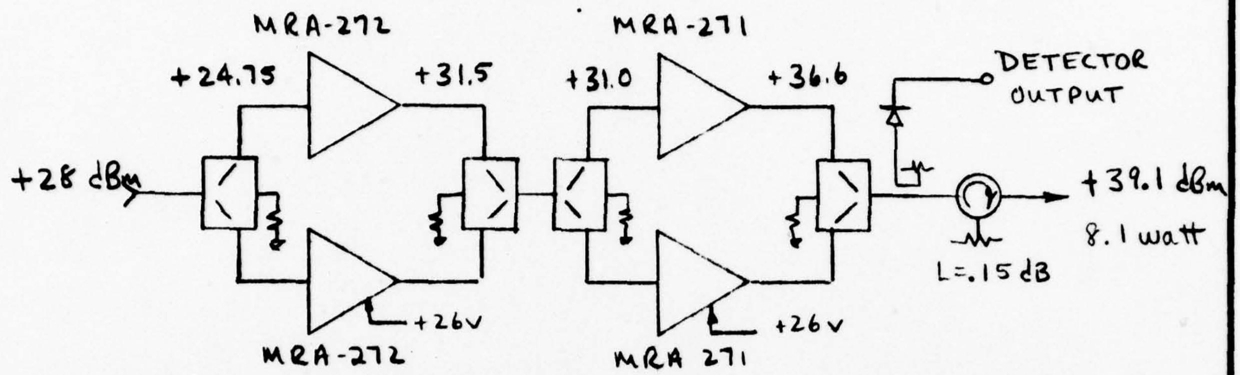
A summary of the expected performance of the two devices, models MRA-271 and MRA-272, is as follows:

	MRA 271	MRA 272
Output Power (Min)	4.5 watts	1.5 watts
Gain (Min)	5 dB	6 dB
Bandwidth	4.4 - 5.0 GHz	4.4 - 5.0 GHz
Efficiency (Min)	20%	20%
Operating Voltage (Max)	26 volt	26 volt
Thermal Resistance (Max)	6^{o}C/Watt	30^{o}C/Watt

Using these transistor specifications, a system block diagram was developed to obtain 100 watts of RF power with 12 Basic Power Modules (BPM's). A block diagram of the BPM is shown in Figure 14. The output power of two MRA 271's is combined to obtain the minimal 8.1 watts required. Two MRA 272's provide the drive required for the power stages. Lange couplers are utilized for power splitting/combining and were included in the interstage section to minimize the difficulties in cascading Class C transistors. Using transistors TRW fabricated from the original lot of devices developed for ECOM, a BPM was built and is shown in Figure 15. The power output versus frequency data shown in Figure 16 identifies several problems found in this design. These include:

BASIC POWER MODULE

USING BIPOLAR TRANSISTORS

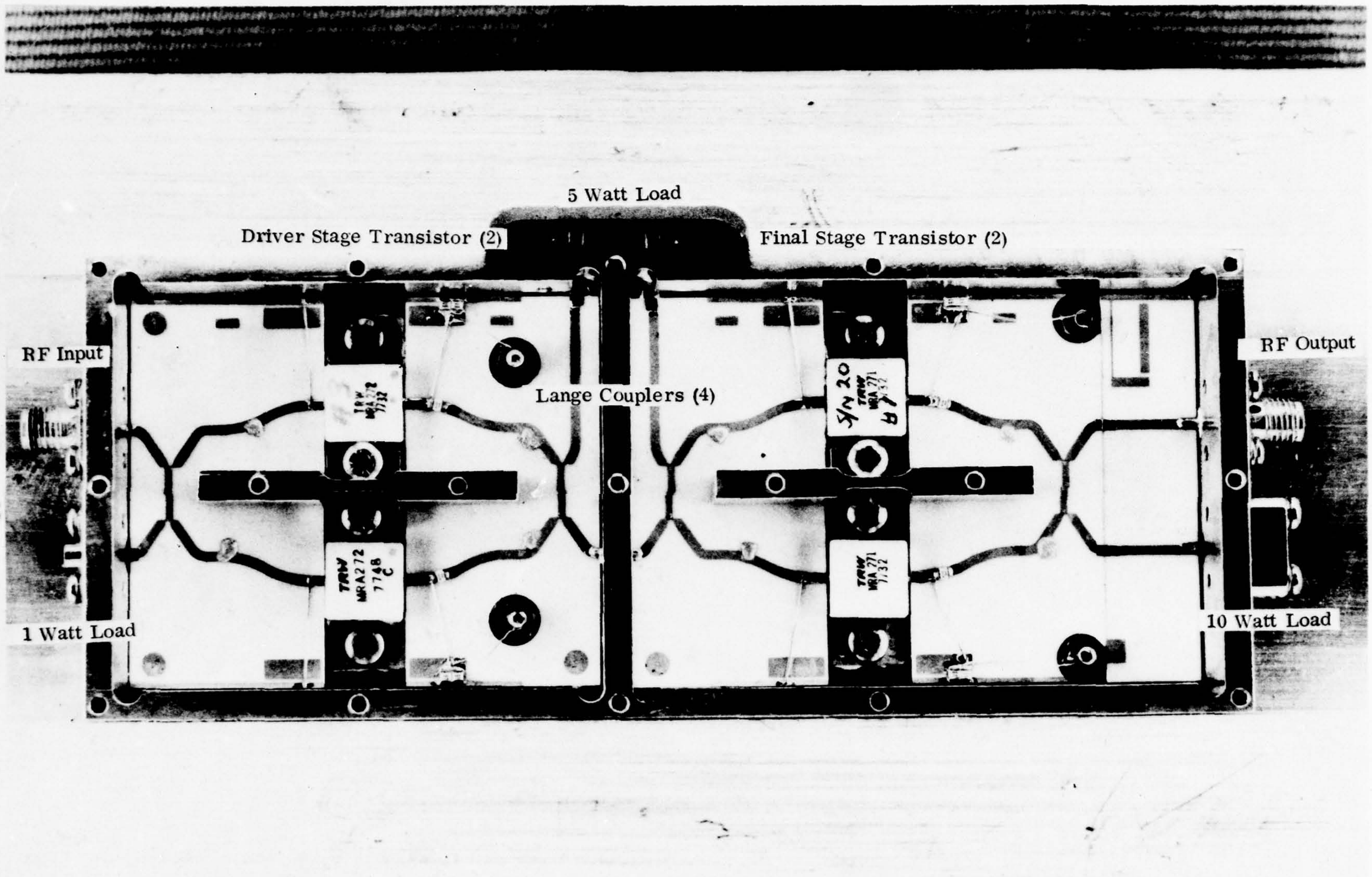


PARAMETER	DESIGN PERFORMANCE
FREQ	4.4 - 5.0 GHz
POUT	+39.1 dBm (8.1 WATT)
PIN	+28 dBm (.63 WATT)
GAIN	11.1 dB
DC POWER	54.4 WATTS (26v at 2.09 amp)
EFFICIENCY	15.1 %

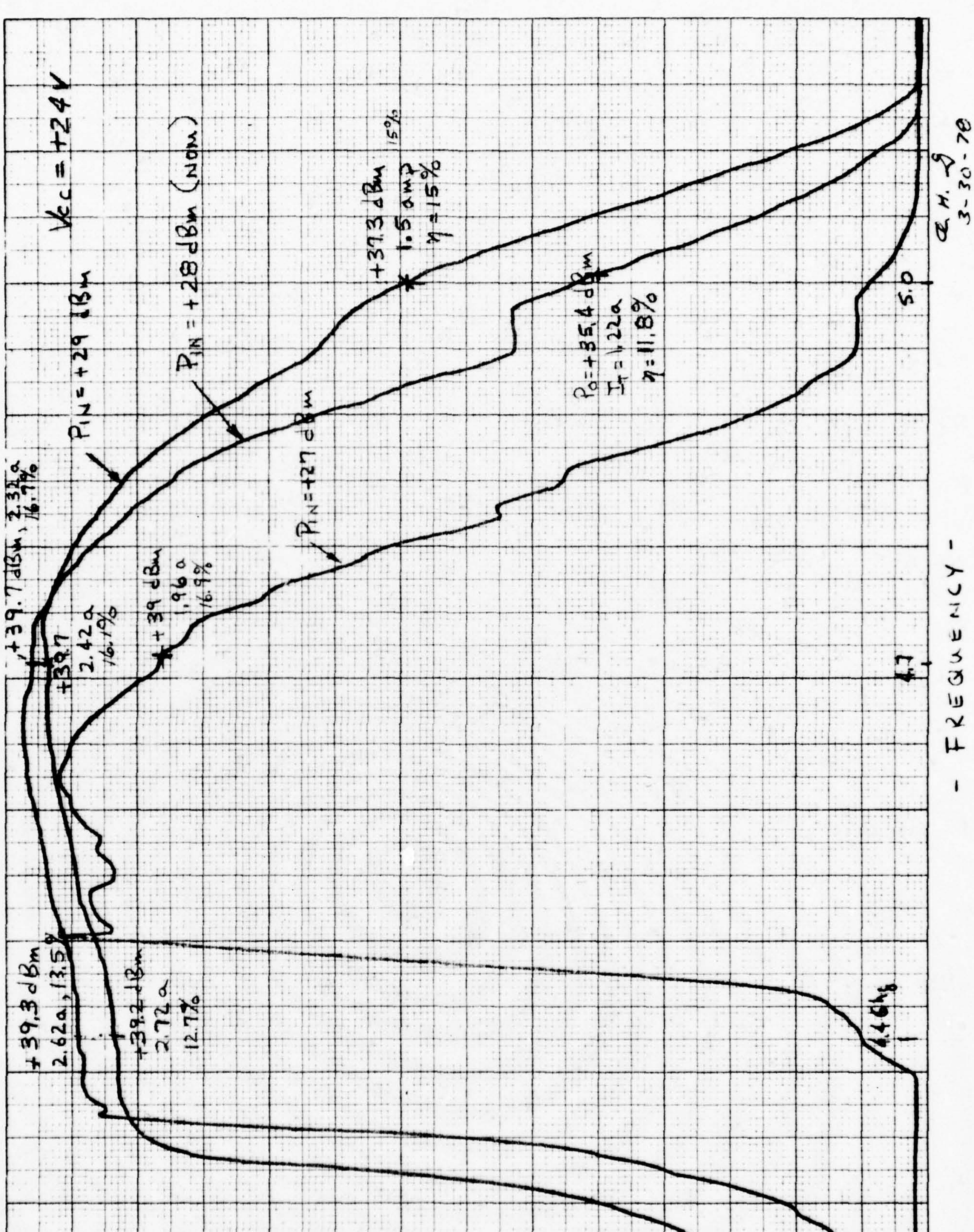
TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION 2 PLACE	3 PLACE	ANGLES	BIPOLAR AMPLIFIER
USED ON	CODE IDENT. NO. 28528	DWG. A SIZE		PHASED ARRAY
PREPARED BY / DATE				
CHECKED BY / DATE				SHEET FIGURE 14

DRAWING NUMBER

ITT DEFENSE COMMUNICATIONS DIVISION
NUTLEY, NEW JERSEY



Silicon Bipolar Transistor Amplifier (BPM)



BIPOLAR BPM

FIGURE 16

- Bandwidth - At the nominal drive level of +28 dBm, the amplifier failed to cover the full 4.4 - 5.0 GHz band. Power output at 5 GHz was 4 dB down from the power obtained at 4.7 GHz.
- Turn-On Characteristics - At a drive level of +27 dBm, 1 dB below nominal, the amplifier response fell off rapidly at both the low and high ends of the frequency band.
- Efficiency - The efficiency of the amplifier was less than required, dropping to less than 13% at 4.4 GHz.

TRW hoped to improve these characteristics on new lots of transistors. Other transistor characteristics considered critical for this application were investigated. These results are summarized below:

Parameter	Measured Results
Phase Tracking (Transistor to Transistor)	23^{o}
AM/PM	10^{o}/dB
Noise Power (100 MHz off carrier)	-136.5 dBm/Hz
Second Harmonic	-28 dBc

Both of the phase characteristics (tracking and AM/PM) were approximately twice the values that were required for a system of this type. Computer calculations of antenna gain and sidelobe levels as a function of random phase and amplitude inputs to the antenna matrix baluns were used to determine the maximum phase and amplitude variations for the BPM's.

The noise power output 100 MHz away from the carrier determines the impact the Phased Array transmitter has upon the AN/GRC-143 receiver. This noise power is coupled into the receiver via coupling between the transmit and receive arrays. With 30 dB isolation between the two arrays, the noise power from the bipolar transistor amplifier results in a calculated noise figure degradation on the order of 4 dB. Receiver noise figure degradation as a function of BPM noise power (dBm/Hz) and antenna isolation is plotted in Figure 17.

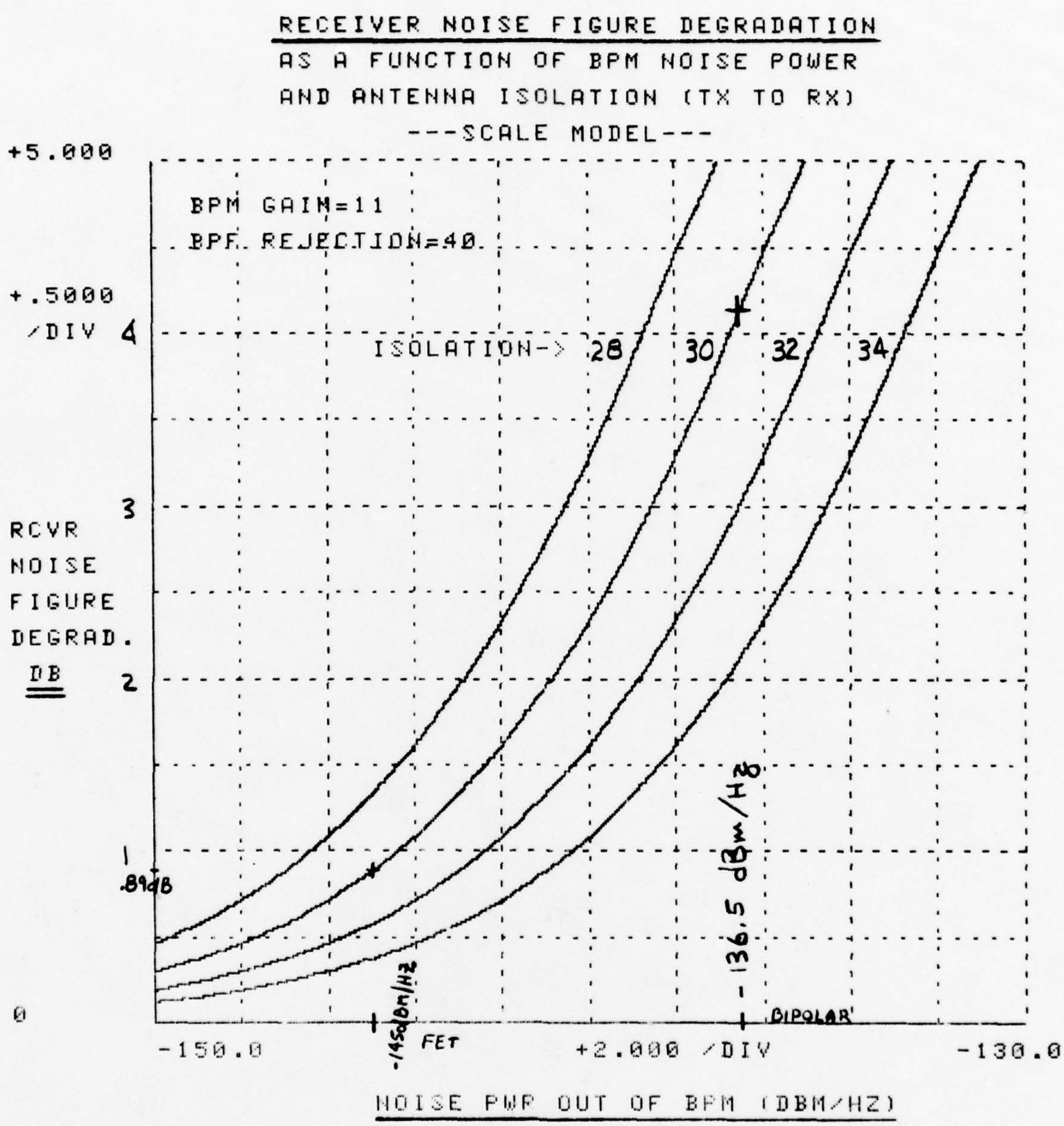

RECEIVER NOISE FIGURE DEGRADATION
AS A FUNCTION OF BPM NOISE POWER
AND ANTENNA ISOLATION (TX TO RX)
---SCALE MODEL---
+5.000
+.5000
/DIV
BPM GAIN=11
BPF REJECTION=40
ISOLATION-> 28 30 32 34
RCVR
NOISE
FIGURE
DEGRAD.
DB
4
3
2
1
.89dB
0
-136.5 dBm/Hz
-145dBm/Hz
FET
BIPOLAR
-150.0
+2.000 /DIV
-130.0
NOISE PWR OUT OF BPM (DBM/HZ)

FIGURE 17

The level of the second harmonic (-28 dBc) indicated that a low pass filter with at least 52 dB rejection at 8.8 GHz would be required at the output of each BPM to meet the spurious radiation specification of -80 dBc.

In summary, measured performance versus design performance for the bipolar was as follows:

	DESIGN	MEASURED
Frequency Range	4.4-5.0	4.4-4.7 GHz
Power Output	8.1 watt	8.5 watt
Gain	11.1 dB	11.3 dB
DC Power	54.5 watt	62.9 watt
Efficiency	15.1%	13.5%
Phase Tracking	10°	23°
AM/PM	$< 5^{\circ}$/dB	10°/dB
Noise Power	-142 dBm/Hz	-136.5 dBm/Hz

Based upon these results, the best projection of system performance using bipolar transistors was as follows:

Frequency	4.5-4.8 GHz
Power Output	100 watts
Efficiency, DC-RF	10%
Duplex Operation	4 dB Noise Figure Degradation

Due to the turn-on characteristics of the bipolar transistors, every loss in the system was critical, particularly the loss of the 12 way power divider and of the interstage Lange couplers. Additional losses of a few tenths of a dB could mean the difference between full output and no output for operation anywhere but band center.

Thus the use of these devices would mean significant shortcomings in evaluating the main system development objectives i.e., bandwidth, efficiency and duplex operation.

The effort with bipolar transistors did not go any further than the building and testing of one BPM. TRW was unsuccessful in its attempts to process any new transistor lots that came close to meeting the requirements for this system application. The decision was made to first investigate an all GaAsFET BPM and based upon that investigation to shift the program from bipolar to FET devices.

GaAsFET Amplifier Results

Several developments forced the Phased Array program to shift to an all GaAsFET approach. These included:

- TRW's lack of success in processing any new bipolar transistor lots to meet the required specifications, even in the small quantities needed for this program.
- The projected Phased Array system performance based upon obtainable bipolar transistors would have been narrow bandwidth (200 - 300 MHz), low efficiency ($<10\%$) and very limited dynamic range.
- The continued improvement in FET power capability with 2.5 watt and 5 watt transistors becoming commercially available during the course of this contract.
- Improvements in FET device processing resulting in high reliability transistors.
- The number of companies actively developing power FET's was much greater than those researching C-Band power bipolar transistors, indicating that FET's would more likely provide the long term solution.

In addition, it was felt that the power FET offered substantial improvements in bandwidth, turn-on, AM/PM, noise power, and efficiency performance.

Disadvantages of the FET included lower power, significantly higher cost and lower operating voltage. A summary of the comparison between bipolar and FET devices using measured data for both devices is as follows:

Transistor Parameter	Bipolar	GaAsFET
Power per Device	4.5 watt*	2.5 watt
Device Efficiency	23%*	27%
Bandwidth	4.5 - 4.8 GHz*	4.4 - 5.0 GHz
AM/PM	10°/dB	3°/dB

*Parameters which are very sensitive to drive level and which negate use of these devices for this system application.

Transistor Parameter	Bipolar	GaAsFET
Turn-On	Class C	Linear
2nd Harmonic	-28 dBc	-38 dBc
Noise Power	-136.5 dBm/Hz	-145 dBm/Hz
DC Power	19.6 W (26v, .75a)	8.5 W (8.5w, 1a)
Package	Non-Hermetic	Hermetic
Cost $/Watt	$90/Watt	$280/Watt

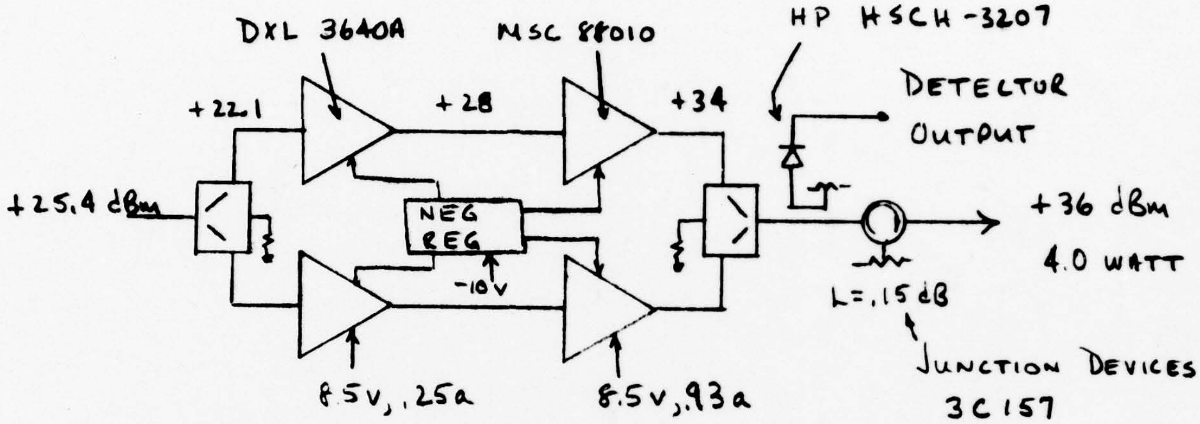
The bipolar cost figure was agreed upon with the device manufacturer for this program only, and does not reflect the true costs (which would be significantly higher). In addition, the development of a Hermetic packaged version of this transistor would add significantly to the device cost. The GaAsFET cost, however, is the current (June, 1979) market price of the Microwave Semiconductor Corporation (MSC) 2.5 watt transistor (MSC 88010). The trends in power FET's indicate rapid price reduction versus time, particularly after competition developes. For example, the MSE 88002 (0.5 watt device) cost $400 when first introduced, but only $150 two years later.

A new system was designed around the commerically available GaAsFET's. The 2.5 watt FET's were used instead of the 5 watt FET's because they were more readily available and less expensive.

BPM - The block diagram of the GaAsFET amplifier is shown in Figure 18. Two MSC 88010 FET's are combined to obtain the nominal 4 watts output power. Drive for the high power FET is provided by a DXL 3640A FET. Power splitting/combining is accomplished with Lange couplers (fabricated on .050" Alumina substrates). Since the FET's operate in a saturated linear mode, no interstage combining/splitting was required. An output isolator is included to minimize the effects of cable and transmit balun VSWR. A detector is also provided for Built In Test Equipment (BITE) circuitry. A photo of the FET BPM is shown in Figure 19.

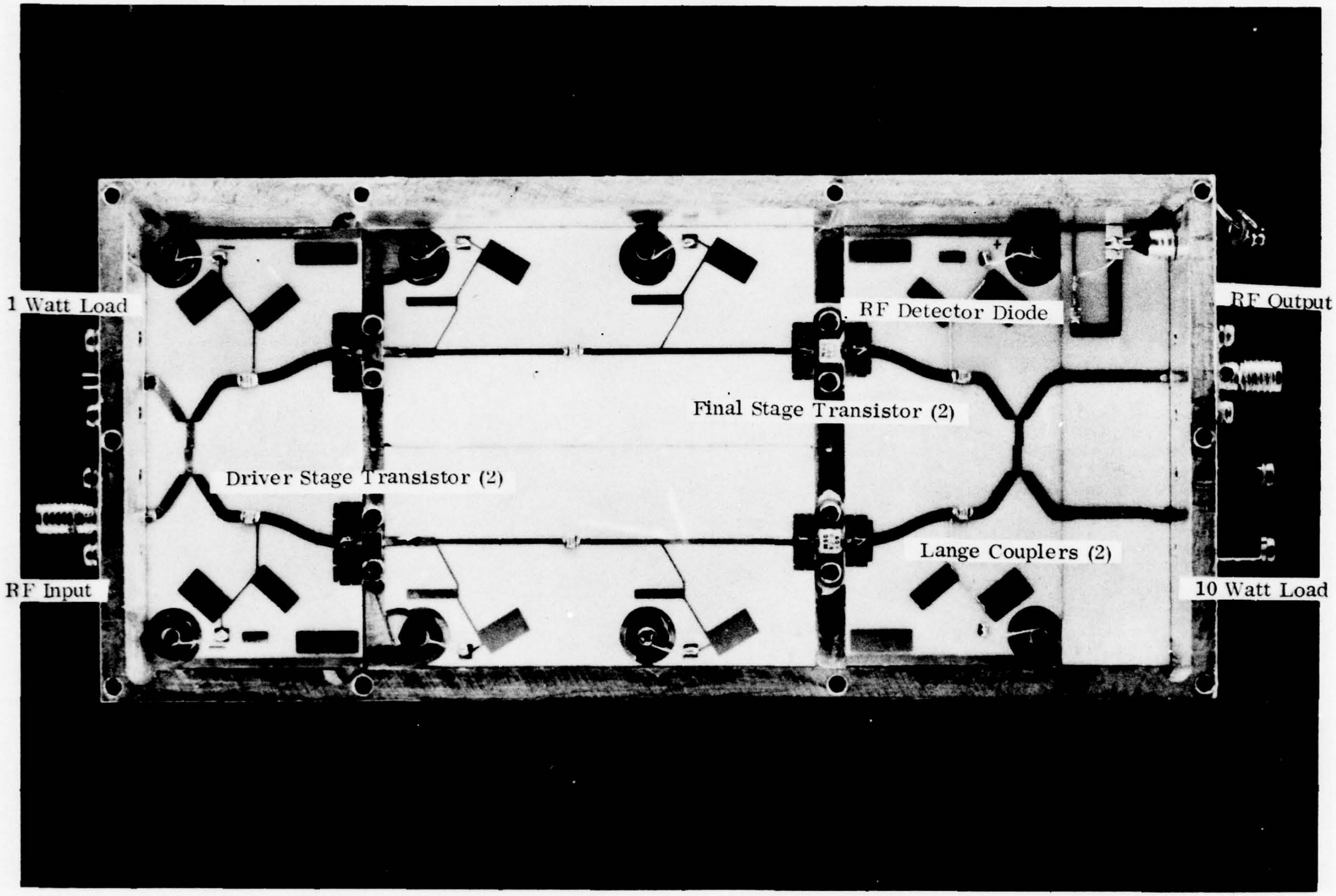
BASIC POWER MODULE

GaAs FET's



FREQ	4.4-5.0 Ghz
POUT	+36 dBm (4 watts)
PIN	+25.4 dBm
Gain	10.6 dB
DC Power	20 WATT (8.5V, 2.35 amp)
EFFICIENCY	20%

TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION 2 PLACE	DECIMAL DIMENSION 3 PLACE	ANGLES	GaAs FET BPM
USED ON		CODE IDENT. NO. 28528	DWG. A SIZE	
PREPARED BY	DATE			
CHECKED BY	DATE			SHEET Figure 18



Gallium Arsenide FET Amplifier (BPM)

A negative voltage regulator is included to provide the required gate voltages for the FET's. The gate voltage on each FET is adjusted to obtain the desired drain current (200 ma for the DXL 3640A, 900 ma for the MSC 88010).

Power output versus frequency as a function of RF drive for one of the FET BPM's is shown in Figure 20. As expected for a linear amplifier, the frequency response is maintained at lower drive levels, greatly enhancing the graceful degradation characteristics of the system. Power output and efficiency as a function of input drive at three frequencies is plotted in Figure 21. BPM efficiencies on the order of 22% were achieved across the entire frequency range. The results obtained from the other BPM's as well as some extended testing results are included in Appendix A. Highlights of this testing follows.

Second harmonic content was measured to be -38 dBc worst case. With the 50 dB rejection provided by the low pass filter, the radiated spurious are more than 88 dB below the carrier. (Spec: -80 dBc)

The third order intercept point was measured to be +45.6 dBm.

Phase characteristics of the BPM's were also investigated. AM/PM conversion was measured to be less than 3^{o}/dB for all three amplifiers, this is comparable to a typical Klystron Tube. Phase tracking measurements (BPM to BPM) indicated a worst case variation of 46^{o}. Two of the amplifiers tracked quite well, being within 15^{o} of each other. The third (BPM #2) had significantly different transmission phase characteristics. This phase variation is believed to be due to a difference in RF matching.

Noise power measurements on the three BPM's indicated a worst case noise power of -86 dBm in a 775 KHz bandwidth (-145 dBm/Hz) at a drive level of +25.4 dBm. This results in a calculated receiver noise figure degradation of 0.89 dB for 30 dB transmit to receive array isolation (See Figure 17).

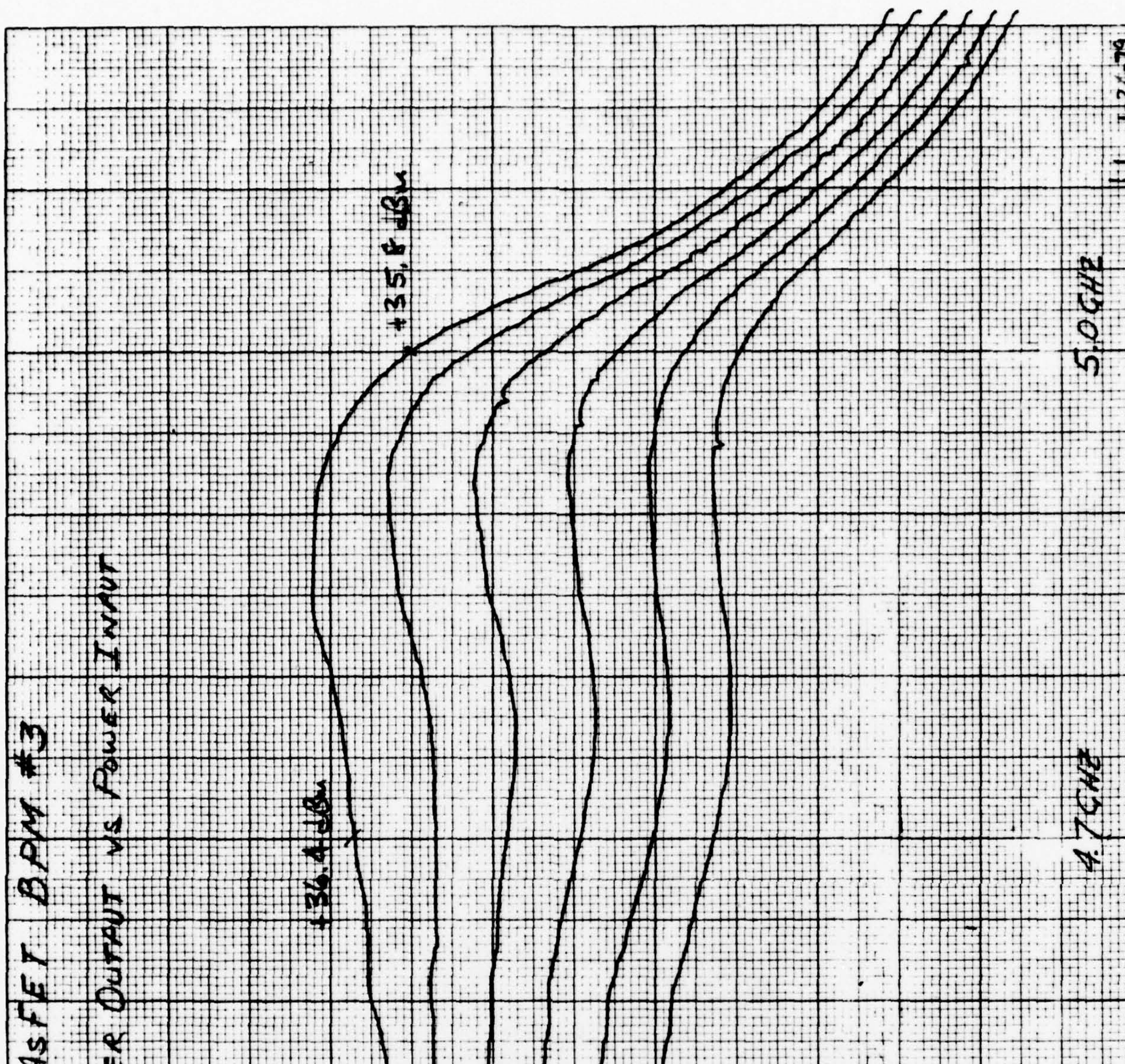

GaAsFET BPM #3
POWER OUTPUT vs POWER INPUT
+36.0 dBm
+36.4 dBm
+35.8 dBm
POWER INPUT
+25.4 dBm
-1dB
-2dB
-3dB
-4dB
-5dB
4.4 GHZ
4.7 GHZ
5.0 GHZ
FREQ - GHz
OUTPUT POWER

FIGURE 20

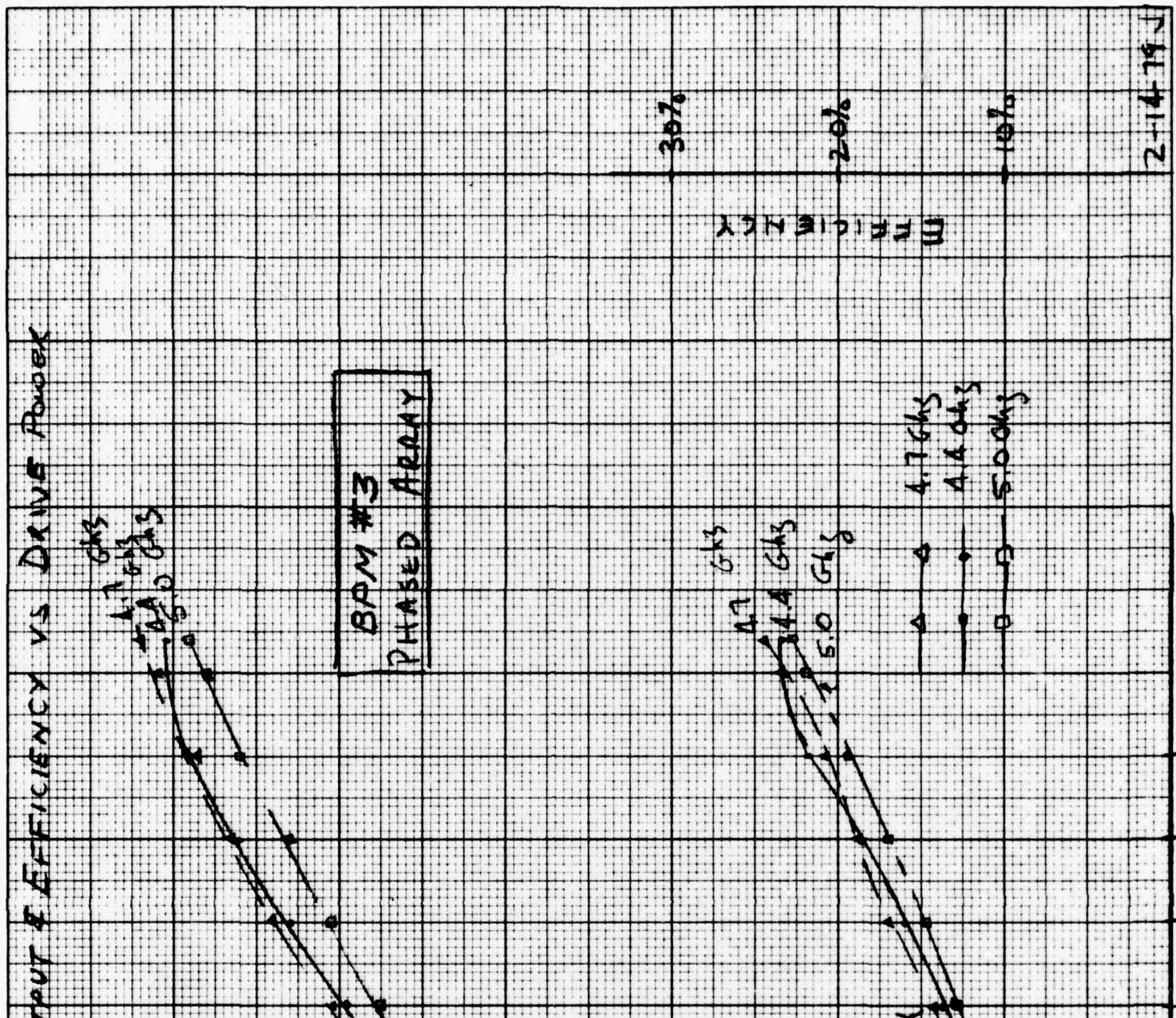

POWER OUTPUT & EFFICIENCY VS DRIVE POWER
BPM #3
PHASED ARRAY
POWER OUTPUT [dBm]
POWER INPUT [dBm]
EFFICIENCY
Power Output
Efficiency
4.7 GHz
4.4 GHz
5.0 GHz
30%
20%
10%
2-14-79 J

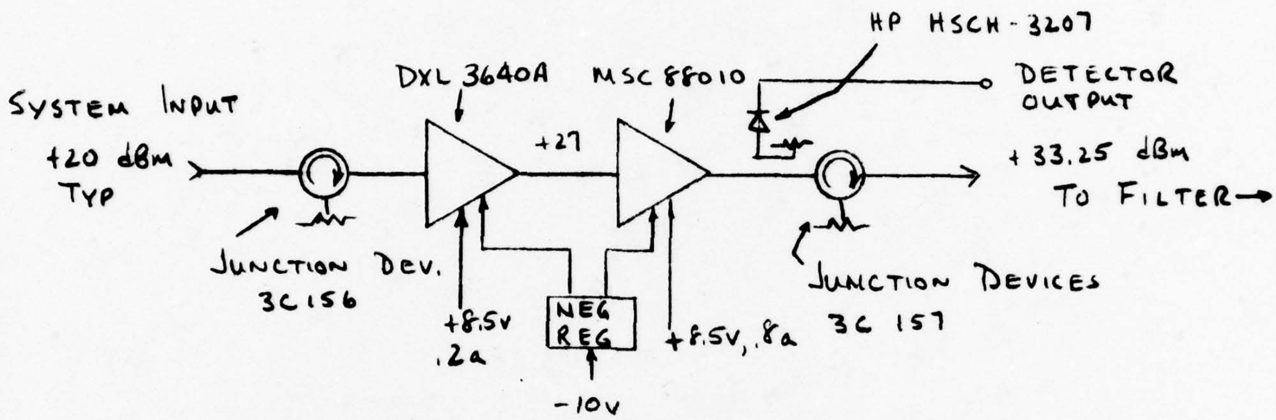
FIGURE 21

Details of these results are included in Appendix A, Part I.

IPA (Intermediate Power Amplifier) - An GaAsFET IPA was also designed, built, and tested to complete the system requirements. This unit is essentially half of a BPM, consisting of a single DXL 3640A driving an MCS 88010 FET. A block diagram of the amplifier is shown in Figure 22. Input and output isolators provide the required system input VSWR and protect against post filter misalignment. A diode detector is included to monitor IPA output power and provide a front panel meter indication. Amplifier matching circuitry is realized on .025" alumina substrates.

The power output of the IPA versus frequency as a function of RF drive is shown in Figure 23. Saturation and efficiency performance is plotted in Figure 24.

INTERMEDIATE POWER AMPLIFIER



FREQ	4.4-5.0 Ghz
POUT	+33.25 dBm
PIN	+20 dBm
Gain	13.25 dB
DC POWER	8.5 watt (8.5v, 1amp)
Efficiency	23%

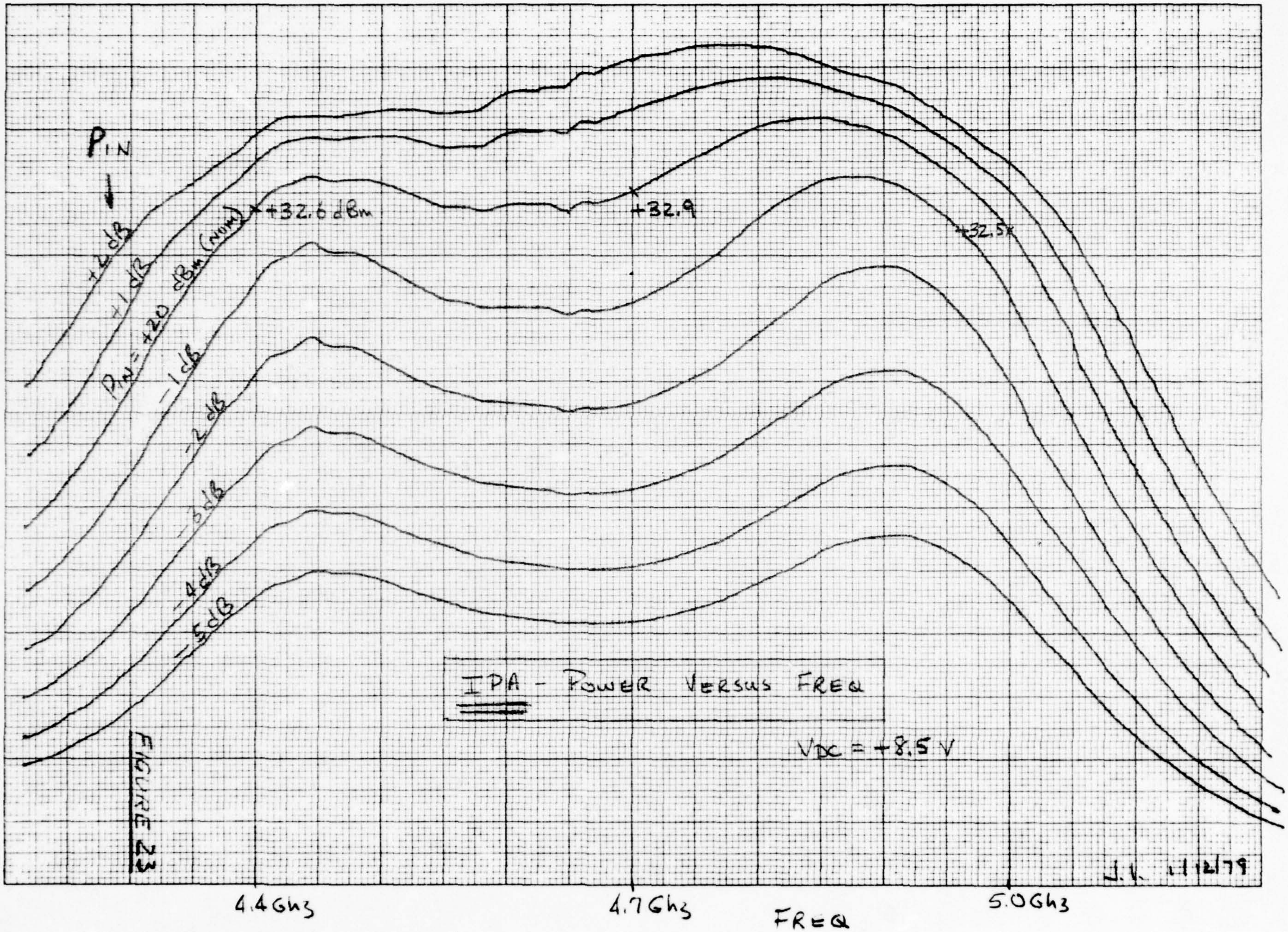
DRAWING NUMBER

ITT DEFENSE COMMUNICATIONS DIVISION — NUTLEY, NEW JERSEY

TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION 2 PLACE	3 PLACE	ANGLES	IPA

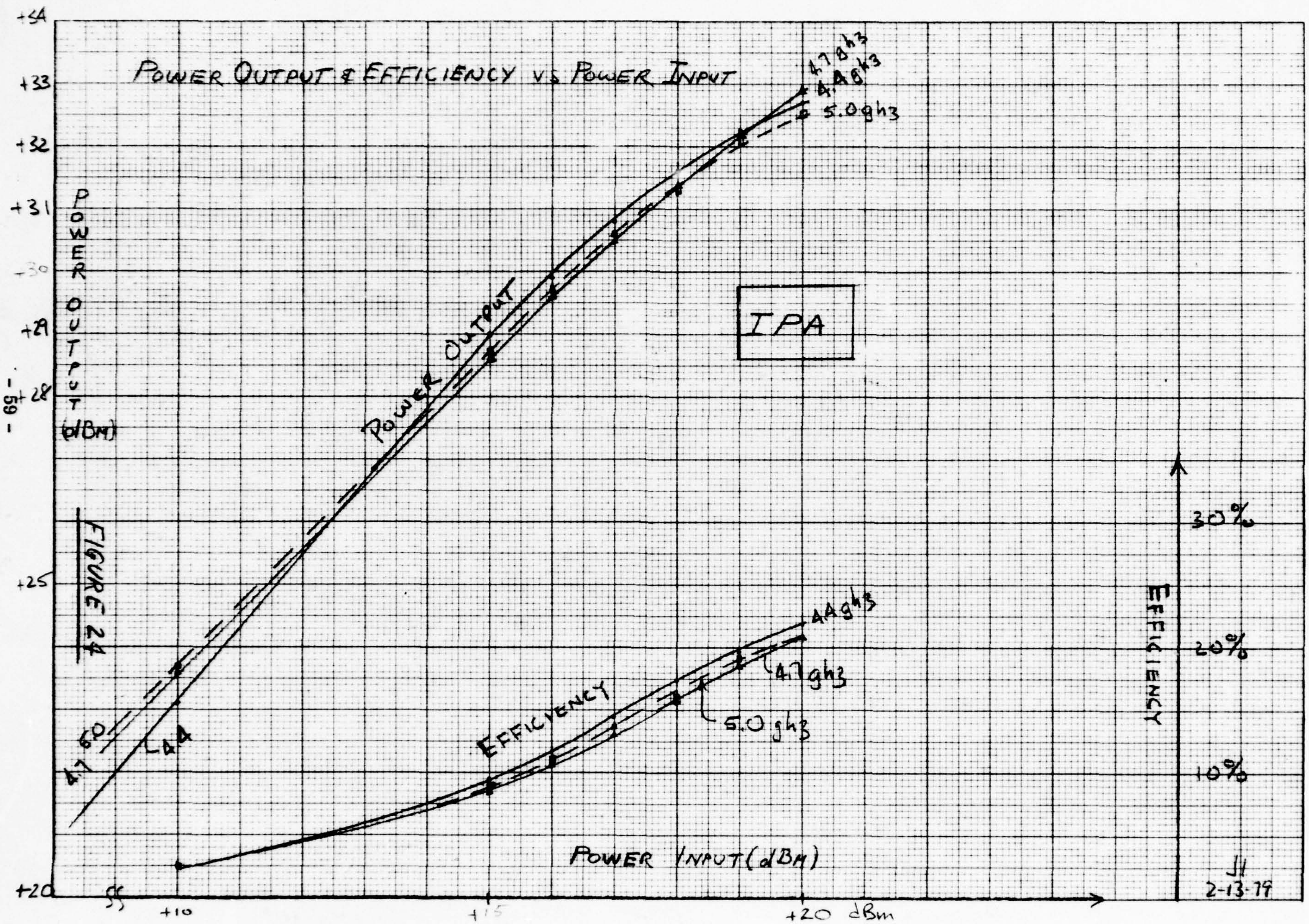
USED ON	CODE IDENT. NO.	DWG. SIZE	
PREPARED BY / DATE	28528	A	PHASED ARRAY
CHECKED BY / DATE			SHEET FIGURE 22

D5215 A REV. 5/73



IPA - POWER VERSUS FREQ
VDC = +8.5 V
PIN
+2 dB
+1 dB
PIN = +20 dBm (NOM)
-1 dB
-2 dB
-3 dB
-4 dB
-5 dB
+32.6 dBm
+32.9
+32.5
4.4Ghz
4.7Ghz
5.0Ghz
FREQ
OUTPUT POWER
J.V. 1/12/79

FIGURE 23



POWER OUTPUT & EFFICIENCY vs POWER INPUT
IPA
POWER OUTPUT (dBm)
POWER OUTPUT
EFFICIENCY
POWER INPUT (dBm)
+20 dBm
+15
+10
+20
+25
+28
+29
+30
+31
+32
+33
+34
4.7 ghz
4.4 ghz
5.0 ghz
30%
20%
10%
JH
2-13-79

FIGURE 24

Passive Components

I) Isolators

The isolators used in the Phased Array system are low loss designs from the Junction Devices Company. The three different model numbers required in the system reflect different connectors and power ratings of the built in terminations. A summary of the measured data on these devices follows:

Model	Where Used	Ins Loss*	VSWR	Isolation
3C157	Amplifier Output	.18 dB	1.15:1 max	25 dB min
3C156	IPA Input	.19 dB	1.2:1 max	25 dB min
3C163	Antenna Input	.19 dB	1.15:1 max	30 dB min

*Maximum loss, 4.4 - 5.0 GHz

II) Low Pass Filters

Low pass filters are required on the output of each BPM to attenuate the second harmonic below the -80 dBc specified level. These filters are 9 pole, coaxial designs provided by Uniform Tubes to the following specifications:

	Specification	Measured
Cutoff Frequency	5.0 GHz	5.0 GHz
Passband Loss	0.4 dB max	.31 dB
Passband VSWR	1.35:1 max	1.27:1 max
Minimum Loss @ $f \geq 8.8$ GHz	50 dB	49.5 dB
Transmission Phase (Unit to Unit)	$\pm 5^{o}$	$\pm 2^{o}$

The measured data on one of these LPF's from 4 to 10 GHz is shown in Figures 25, 26, & 27. Maximum passband VSWR for this unit measured 1.20:1 at 5.0 GHz. The next two plots are of insertion loss, the second being a expanded scale showing passband loss in detail. Maximum passband loss was measured to be 0.284 dB at 5.0 GHz with a minimum loss of 49.6 dB at frequencies above 8.8 GHz.

III) 3 dB Hybrids

Two types of 3 dB hybrids are required in the Phased Array amplifier matrix. Quadrature hybrids are utilized in the BPM's for power splitting and combining.

VSWR vs FREQUENCY

PHASED ARRAY JAN 31 1979

UNIFORM TUBES LOW PASS FILTERS

UT-L1-250-5000-9

SER # 002

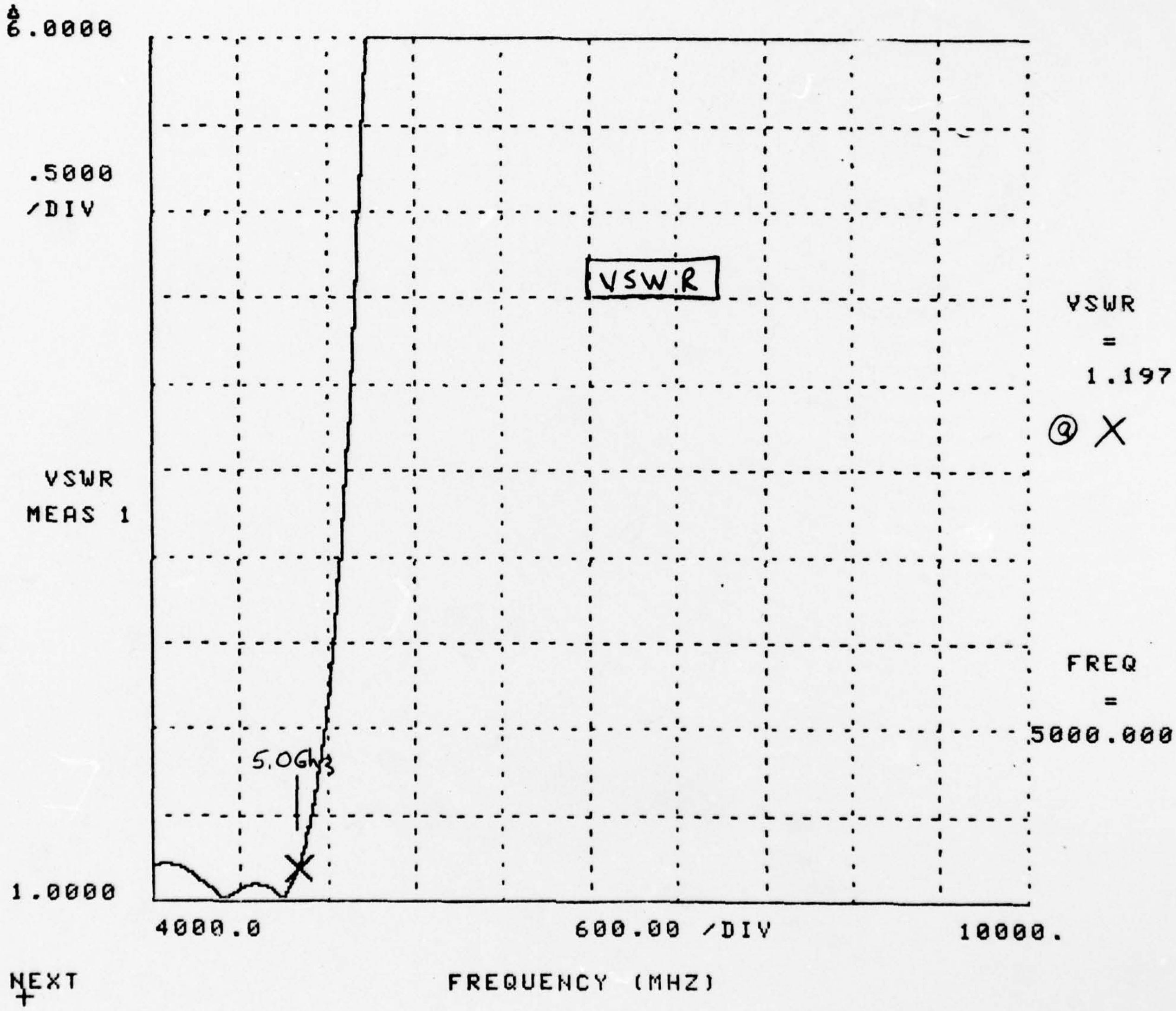


FIGURE 25

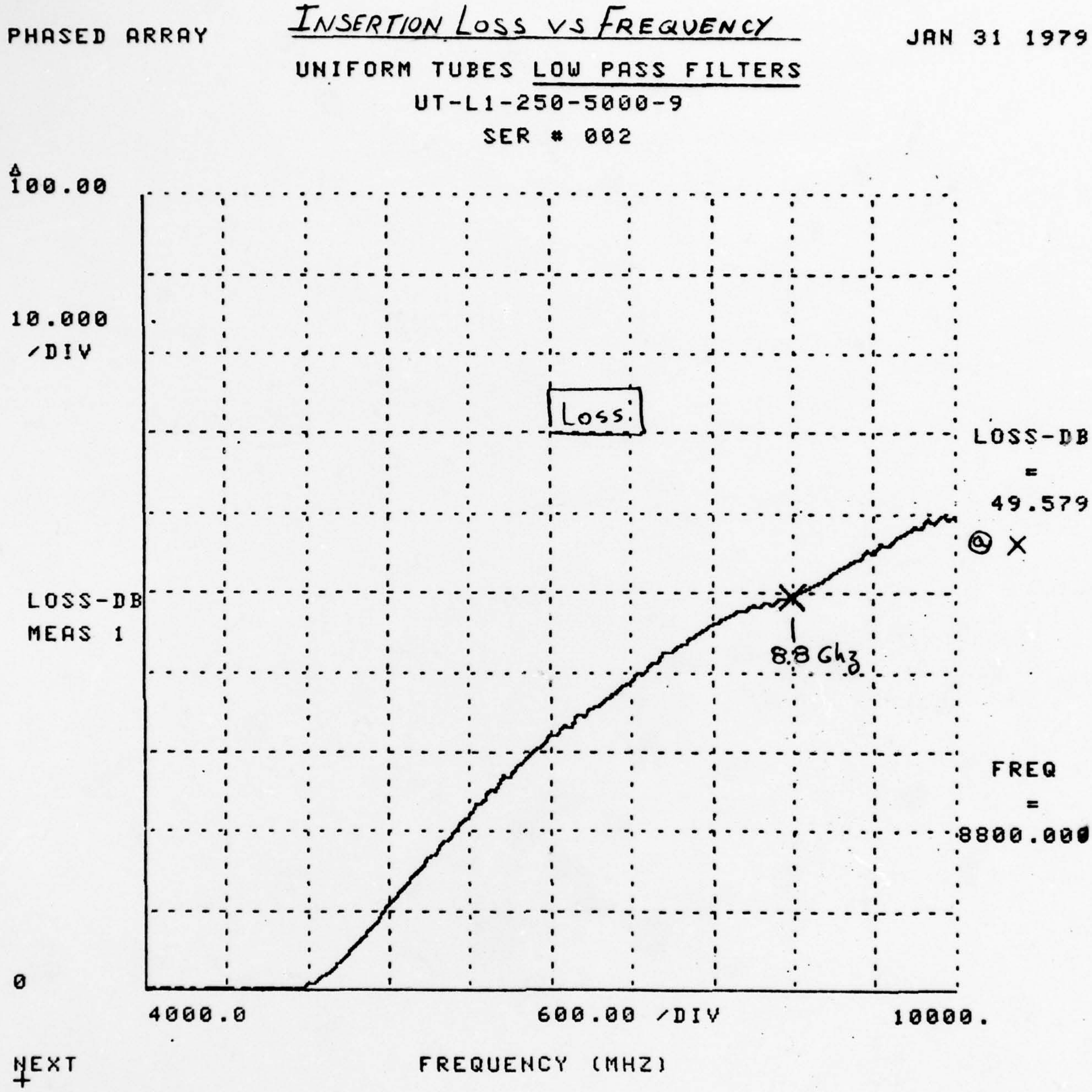

PHASED ARRAY
INSERTION LOSS VS FREQUENCY
JAN 31 1979
UNIFORM TUBES LOW PASS FILTERS
UT-L1-250-5000-9
SER # 002
100.00
10.000
/DIV
Loss:
LOSS-DB
=
49.579
@ X
LOSS-DB
MEAS 1
8.8 Ghz
FREQ
=
8800.000
0
4000.0
600.00 /DIV
10000.
NEXT
FREQUENCY (MHZ)

FIGURE 26

PHASED ARRAY — INSERTION LOSS VS FREQUENCY — JAN 31 1979

UNIFORM TUBES LOW PASS FILTERS

UT-L1-250-5000-9

SER # 002

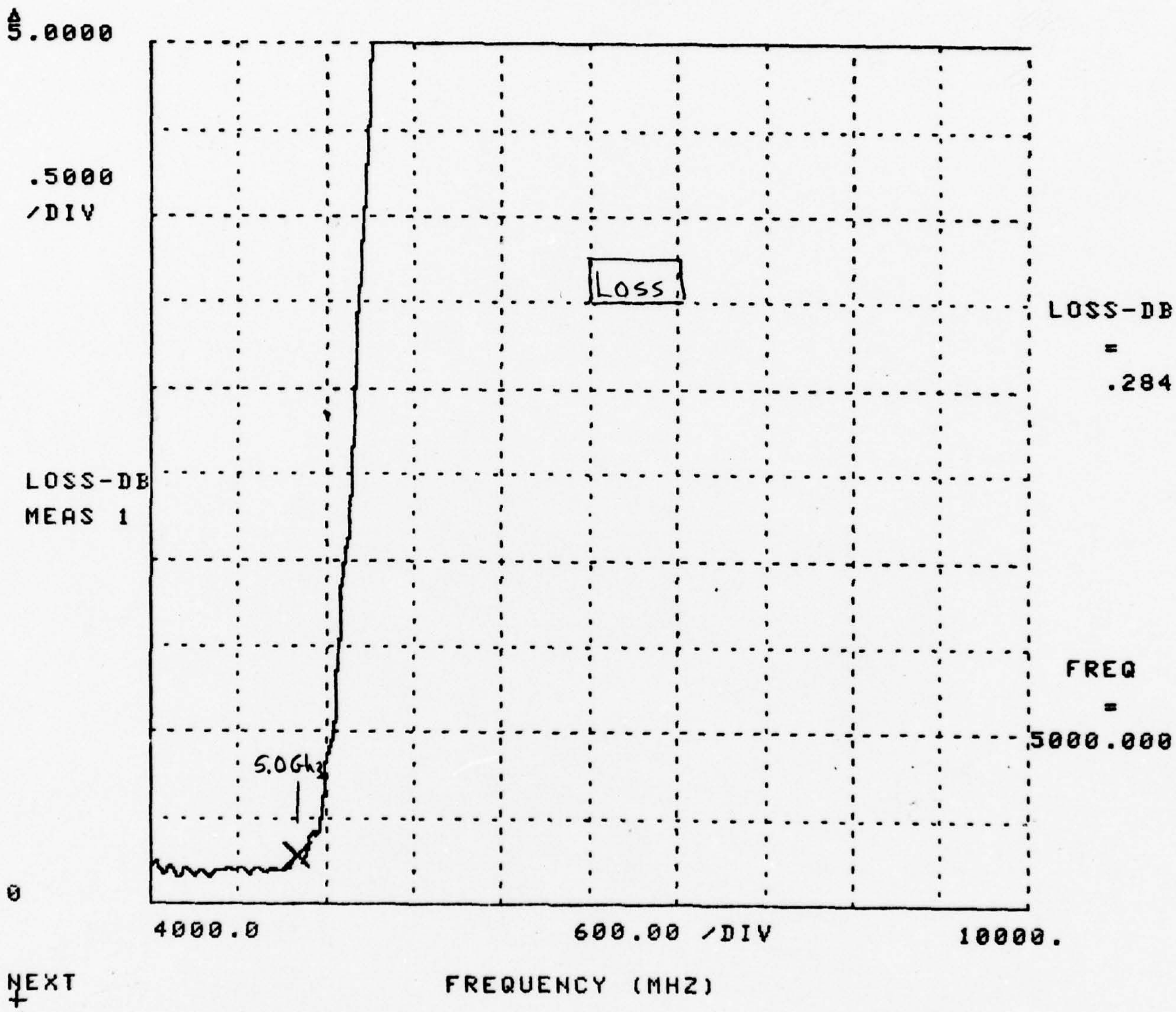


FIGURE 27

The requirements include low loss ($<.25$ dB), large bandwidth and high power handling capability for combining the outputs of two final amplifier stages. The second type of hybrid is an in-phase divider to provide equal phase signals to the transmit baluns. Key requirements on this unit include low loss, phase tracking between outputs and medium power handling capability.

A comparison of the 3 dB hybrids considered for these applications appears in Figure 28 and includes Wilkinson, Branchline , Lange, and Overlay.

For the quadrature hybrid application, the Wilkinson was eliminated because of its low power handling capability. The double Branchline has adequate bandwidth but higher loss. The Overlay design was investigated because of its desirable loss and power characteristics as well as its relative ease of interfacing directly with the microstrip circuitry in the amplifier. These hybrids had tab input and output connections which could be soldered directly to the amplifier circuitry. A high dielectric constant material is required for the microstrip circuitry to minimize the interface problems between the stripline hybrid structure and the microstrip. Alumina ($\epsilon_r = 9.9$) was thus chosen for the amplifier modules (refer to section on substrate material selection).

Despite a considerable effort, this transition from stripline to microstrip radiated and low VSWR transitions could not be obtained.

Lange interdigital couplers were thus selected despite their more difficult fabrication problems. The couplers are fabricated on .050" thick alumina (1" x 2") with gap and line width dimensions of 3.2 mils and 6.8 mils respectively. Measured data on this design is shown in Figures 29, 30, 31, & 32, and is summarized below.

Frequency	4.4 - 5.0 GHz
Insertion Loss	0.3 dB
Amplitude Balance	±0.1 dB max
VSWR	1.21:1 max
Isolation	24 dB min
Phase Balance	$90^{o} \pm 2^{o}$

COMPARISON TABLE

3 dB HYBRIDS 4.4 - 5.0 GHz

	Phase	BW	IL	Isolation (1)	Isolation (2)	Size*	Ease of Fabrication
Wilkinson	0^o	10%	.25 dB	20-30 dB	3 dB	1" X 1"	Easy
Double Wilkinson	0^o	50%	.35 dB	20-40 dB	3 dB	1" X 1.5"	Easy
Branch Line	90^o	8%	.25 dB	20-30 dB	20 dB	1" X 1"	Easy
Double Branch Line	90^o	13%	.35 dB	20-40 dB	20 dB	1" X 1.5"	Easy
Lange	90^o	Octave	.25 dB	20-40 dB	20 dB	.5" X .5"	Difficult
Overlay	90^o	Octave	.25 dB	20-40 dB	20 dB	.4" X 1.2"	Moderate

(1) Output port isolation - input terminated

(2) Input-output isolation with equal output mismatch

* Teflon fiberglass substrate E_R - 2.2

Fig. 28

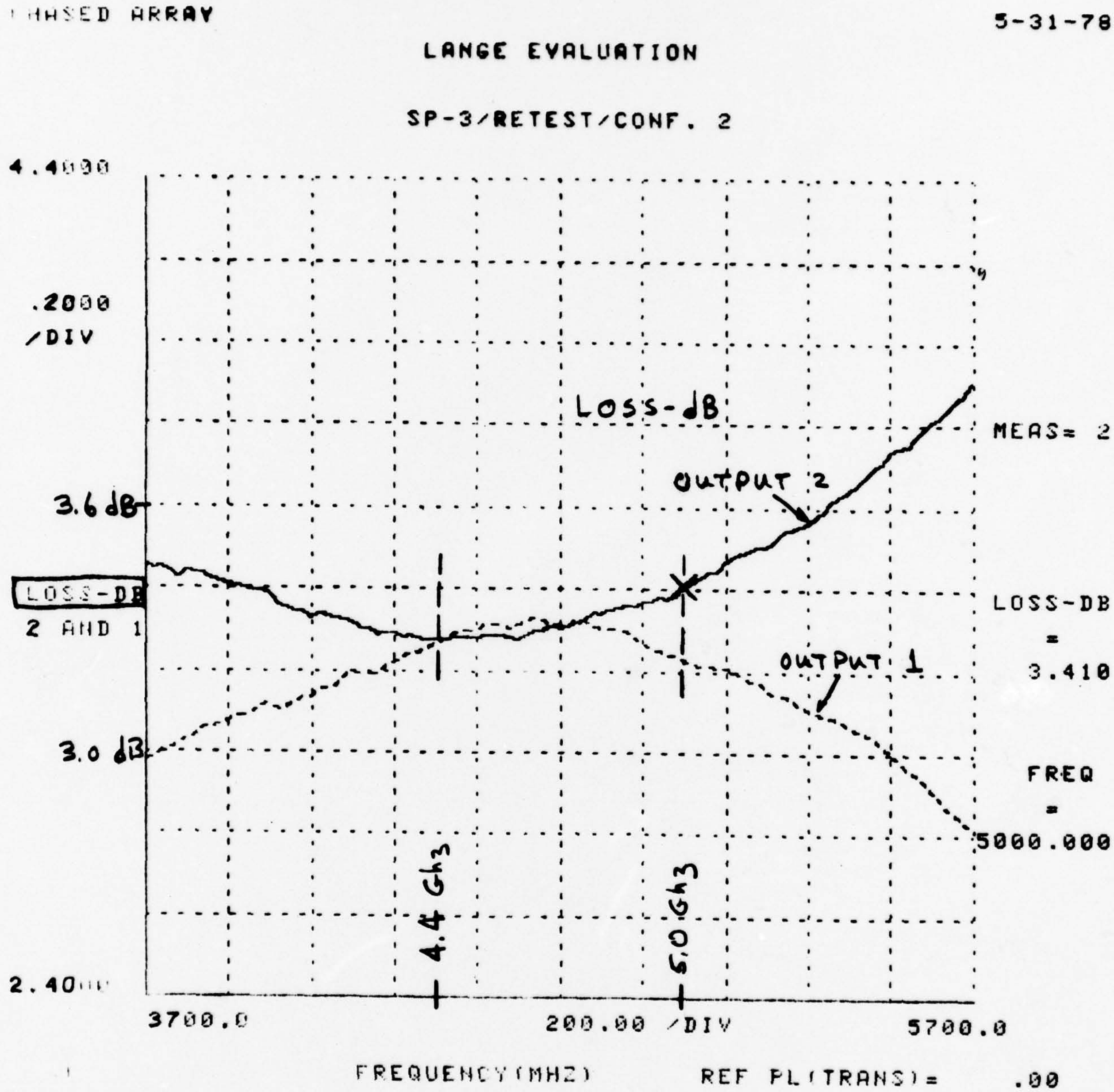
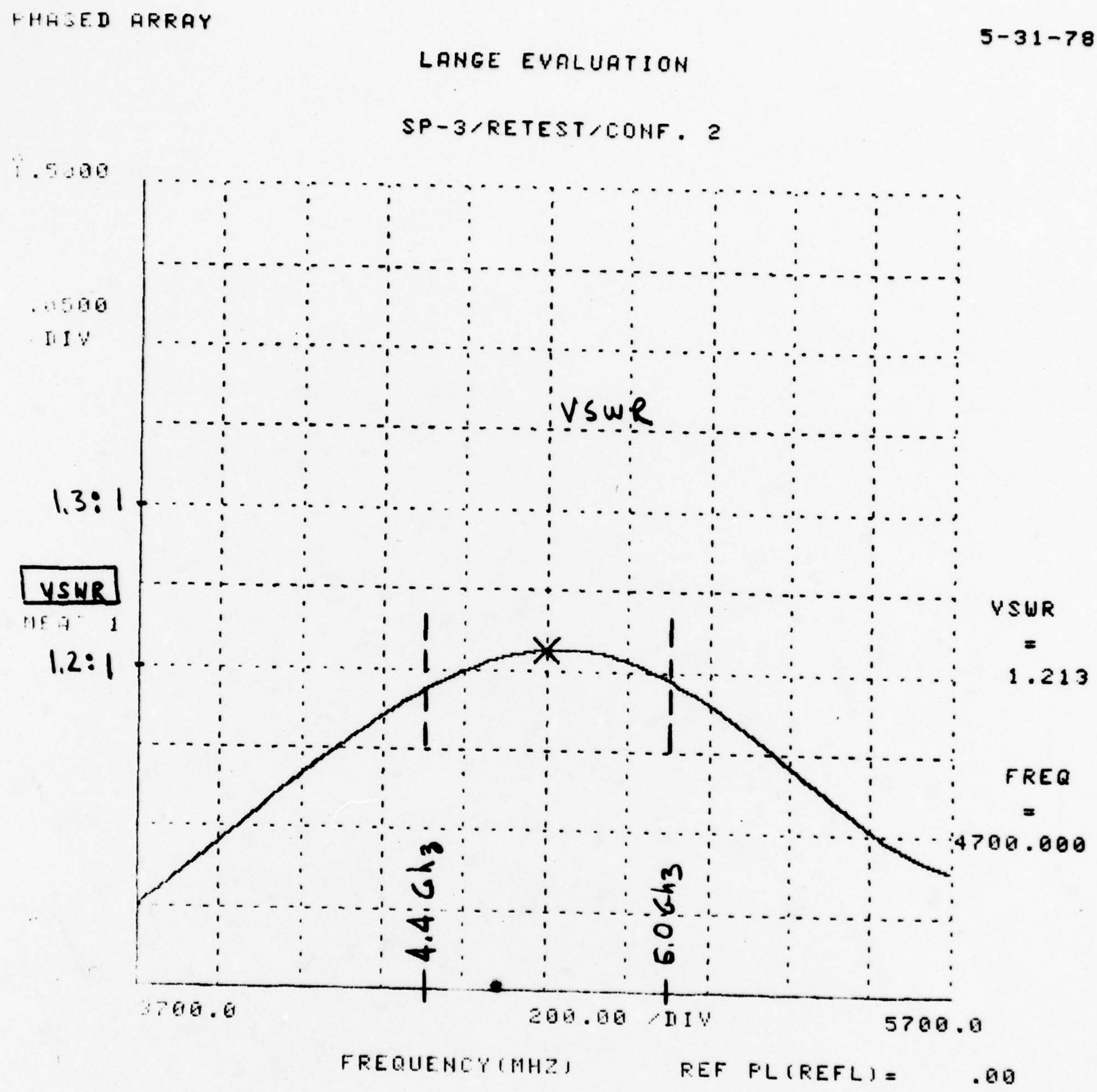

PHASED ARRAY
5-31-78
LANGE EVALUATION
SP-3/RETEST/CONF. 2
4.4000
.2000
/DIV
LOSS-dB
MEAS= 2
OUTPUT 2
3.6 dB
LOSS-DB
2 AND 1
LOSS-DB
=
3.410
OUTPUT 1
3.0 dB
FREQ
=
5000.000
4.4 Ghz
5.0 Ghz
2.4000
3700.0
200.00 /DIV
5700.0
FREQUENCY(MHZ)
REF PL(TRANS)=
.00

FIG 29



PHASED ARRAY
5-31-78
LANGE EVALUATION
SP-3/RETEST/CONF. 2
1.5000
.0500
DIV
VSWR
1.3:1
VSWR
MEAS 1
1.2:1
VSWR
=
1.213
FREQ
=
4700.000
4.4 Ghz
6.0 Ghz
3700.0
200.00 /DIV
5700.0
FREQUENCY (MHZ)
REF PL(REFL) = .00

FIGURE 30

FIGURE 31

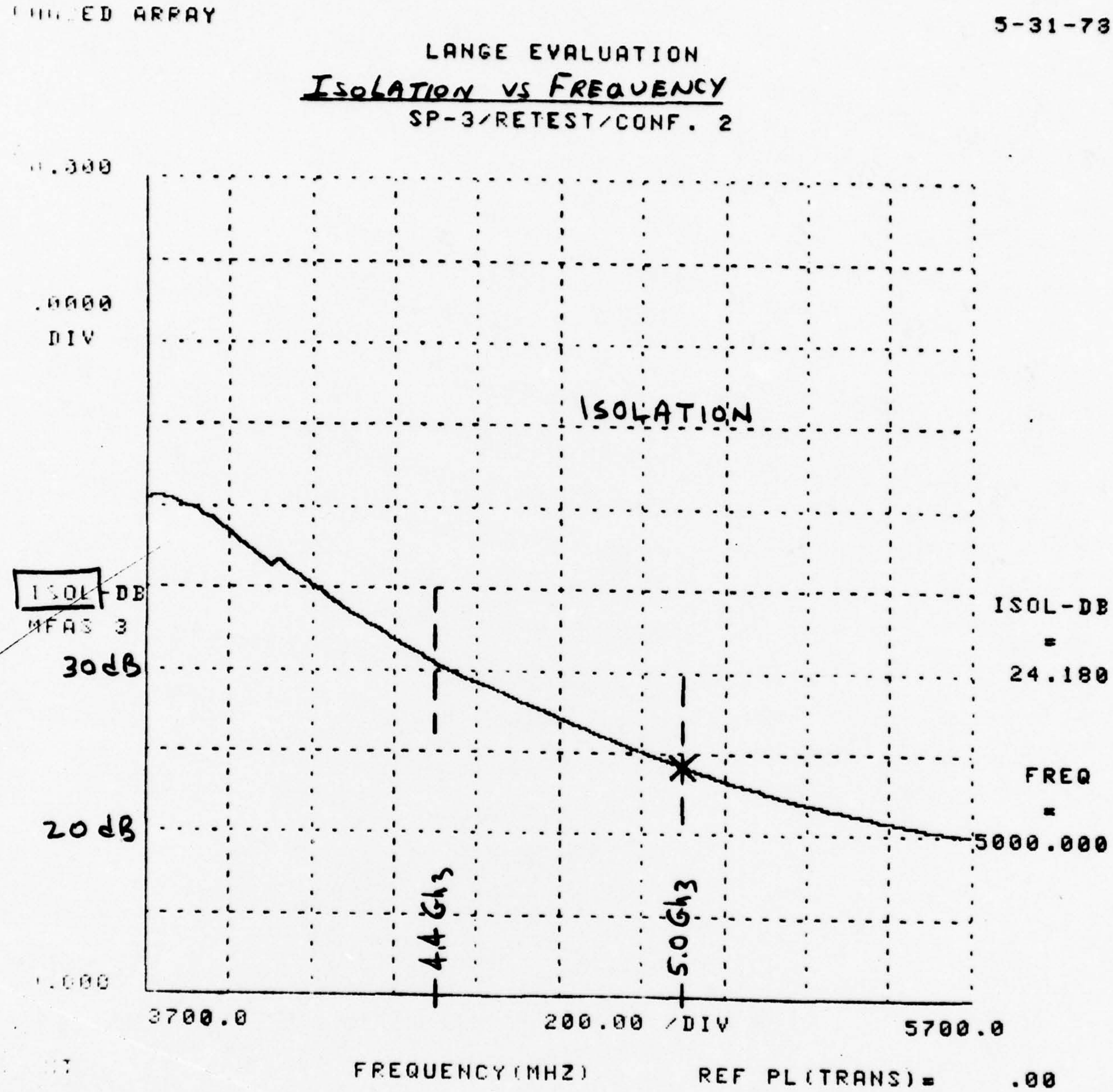


Figure 31

PHASED ARRAY 5-31-78

LANGE EVALUATION

SP-3/RETEST/CONF. 2

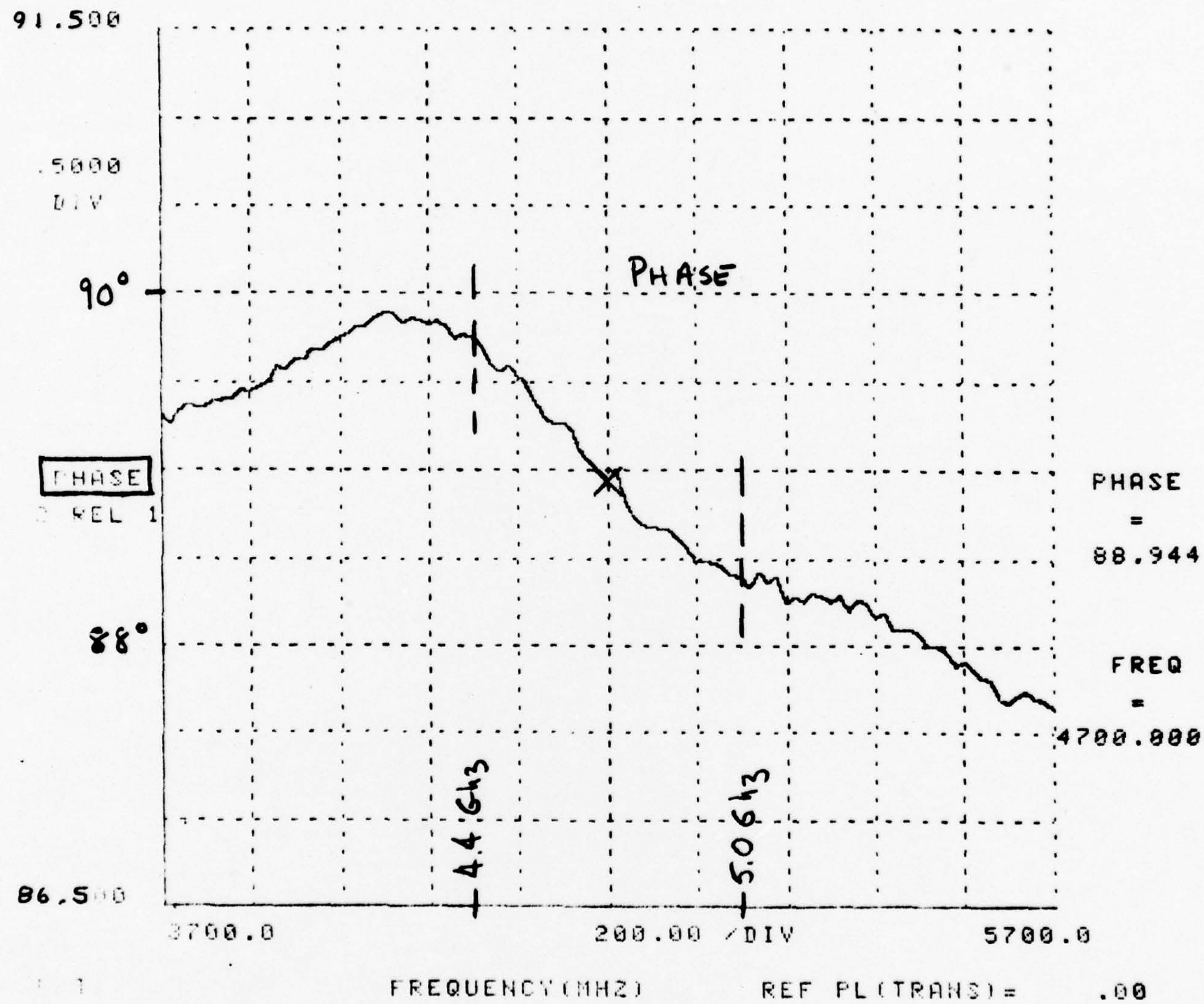


FIGURE 32

The couplers include a considerable amount of 50 ohm line that is required to feed the amplifiers. The 50Ω termination is flange mounted to the amplifier chassis and is rated at 1 watt for the input power splitter and 10 watts for the output combiner.

The in-phase power divider is a commercially available planar Wilkinson design (Merrimac PDM-20-4.76). Measured performance for this unit is shown in Figures 33 thru 36 and is summarized below:

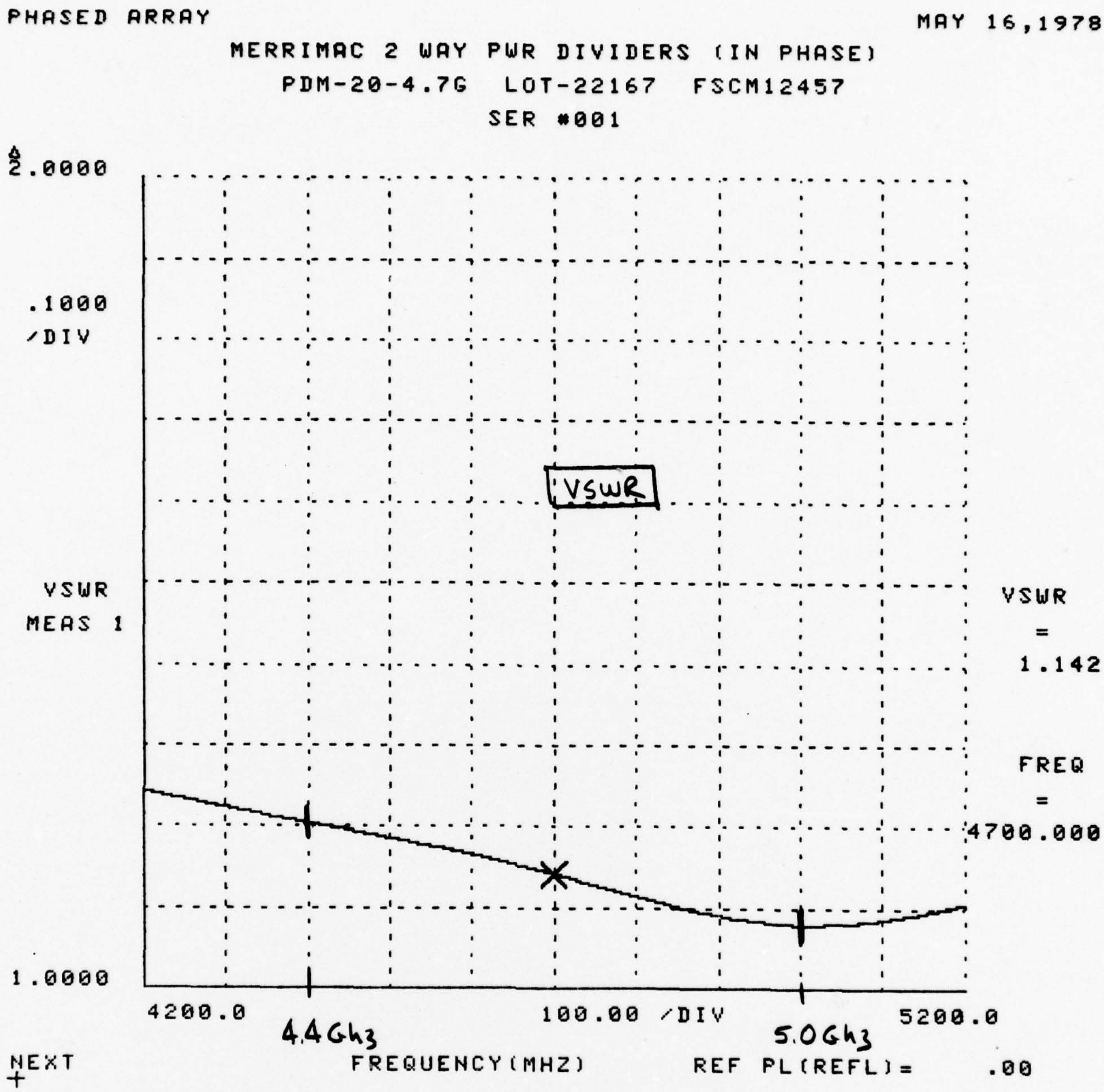
Frequency	4.4 - 5.0 GHz
Loss	0.28 dB max
Amplitude Balance	±.05 dB max
VSWR	1.2:1 max
Phase Blance	±2^{o} max
Isolation	24 dB min

IV. Three Way Power Divider

Three way power dividers are required both in the transmitter portion to provide equal power, equal phase inputs to the BPM's and in the receive array combiner network. These units were designed and built by ITTDCD because the commercially available devices were octave bandwidth designs which were operating near the edge of its frequency band. By designing a divider optimized for the 4.4 - 5 GHz frequency band, substantially improved loss and VSWR performance was obtained.

The power divider is a double section, planar Wilkinson design shown schematically in Figure 37 . The units are stripline construction using .062" thick Duroid substrates with 1 oz Gold plated copper. Measured data on one of these devices appears in Figures 38 thru 42 and is summarized below.

Frequency	4.4 - 5.0 GHz
Input VSWR	1.15:1 max
Loss	0.3 dB max
Amplitude Balance	±0.2 dB
Phase Balance	±5^{o} max
Isolation	20 dB min



PHASED ARRAY
MAY 16,1978
MERRIMAC 2 WAY PWR DIVIDERS (IN PHASE)
PDM-20-4.7G LOT-22167 FSCM12457
SER #001
2.0000
.1000
/DIV
VSWR
MEAS 1
VSWR
=
1.142
FREQ
=
4700.000
1.0000
4200.0
100.00 /DIV
5200.0
4.4Ghz
5.0Ghz
VSWR
NEXT
FREQUENCY(MHZ)
REF PL(REFL)= .00

FIG 33

PHASED ARRAY MAY 16,1978

MERRIMAC 2 WAY PWR DIVIDERS (IN PHASE)

PDM-20-4.7G LOT-22167 FSCM12457

SER #001

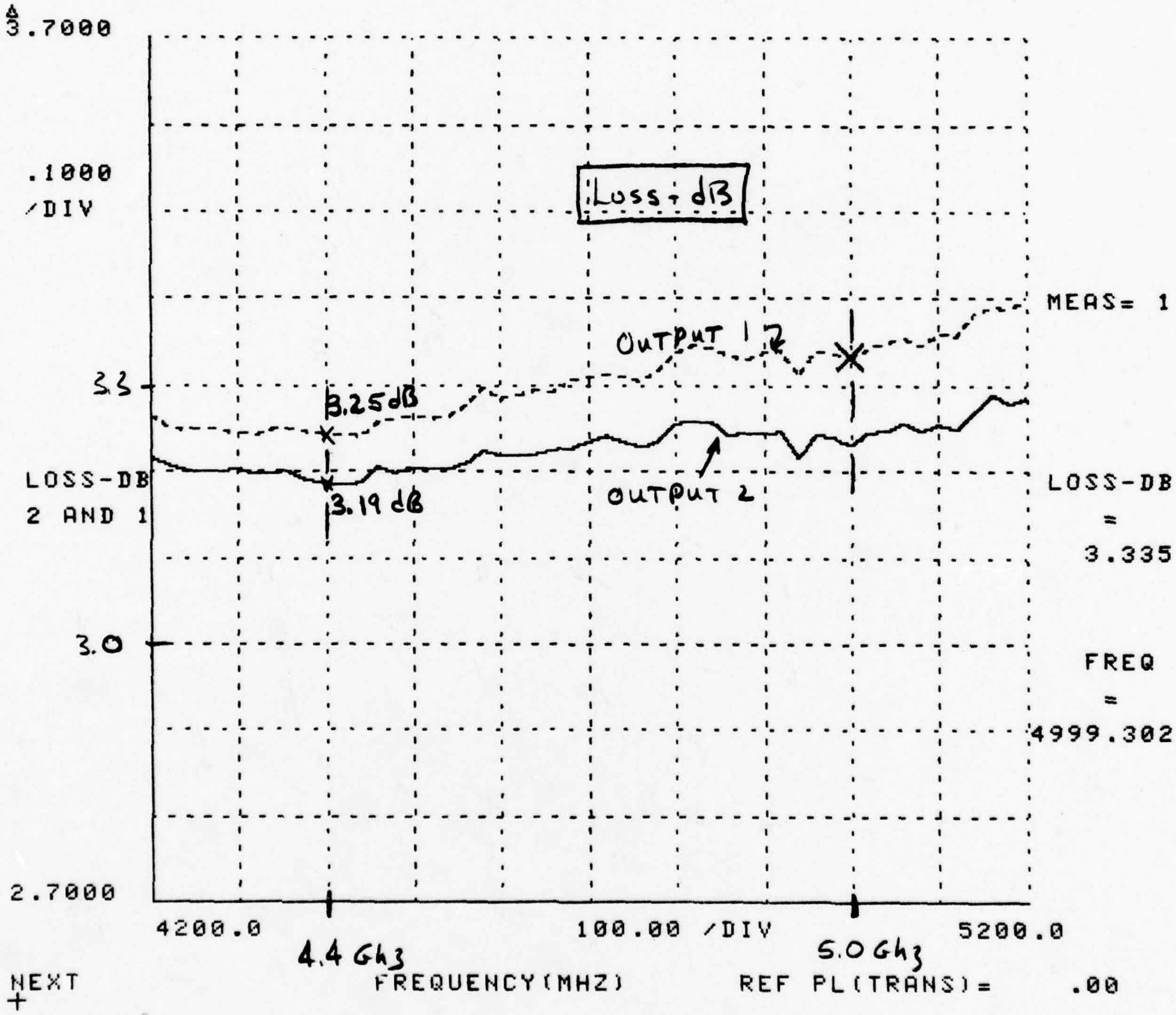
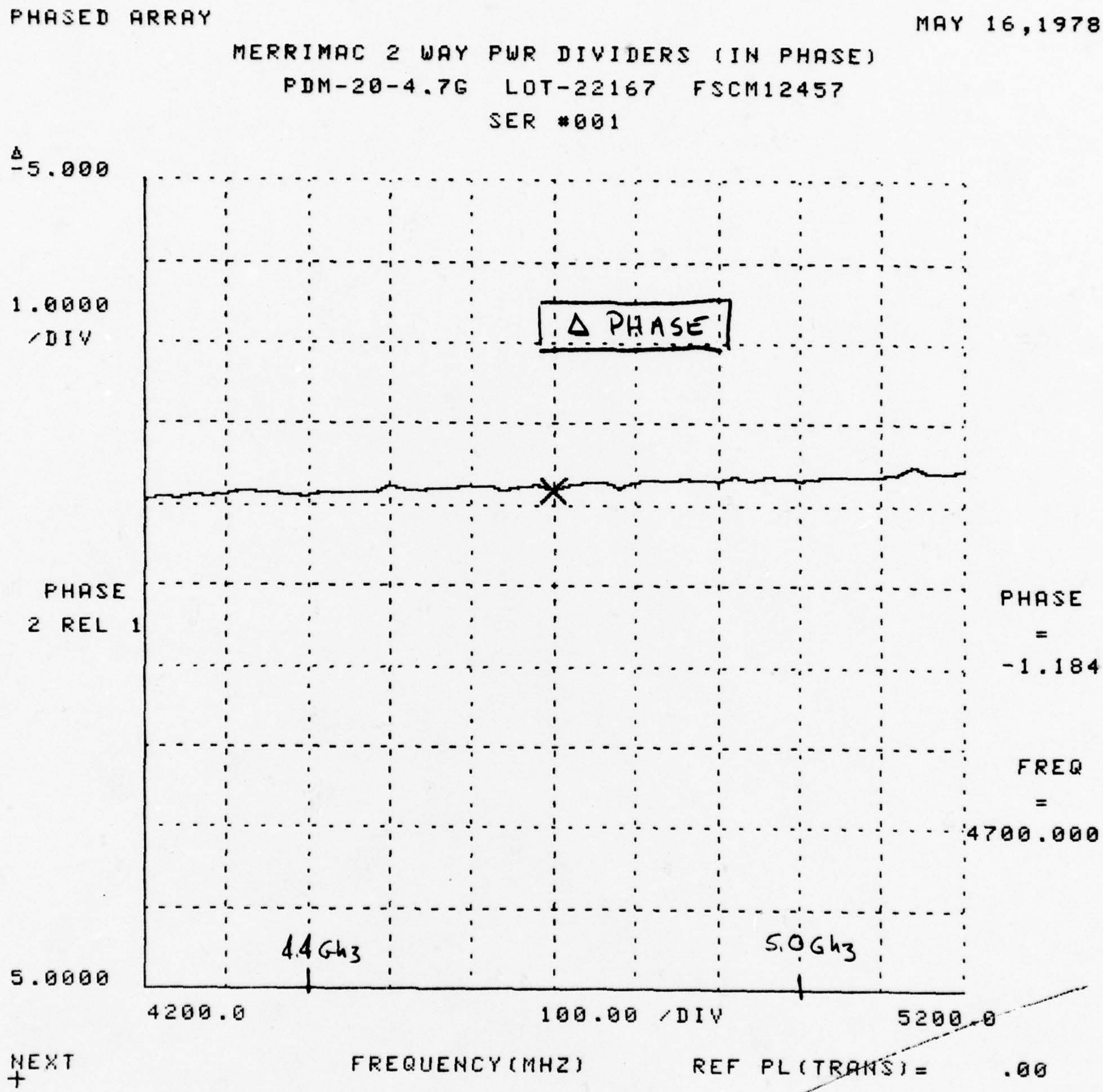
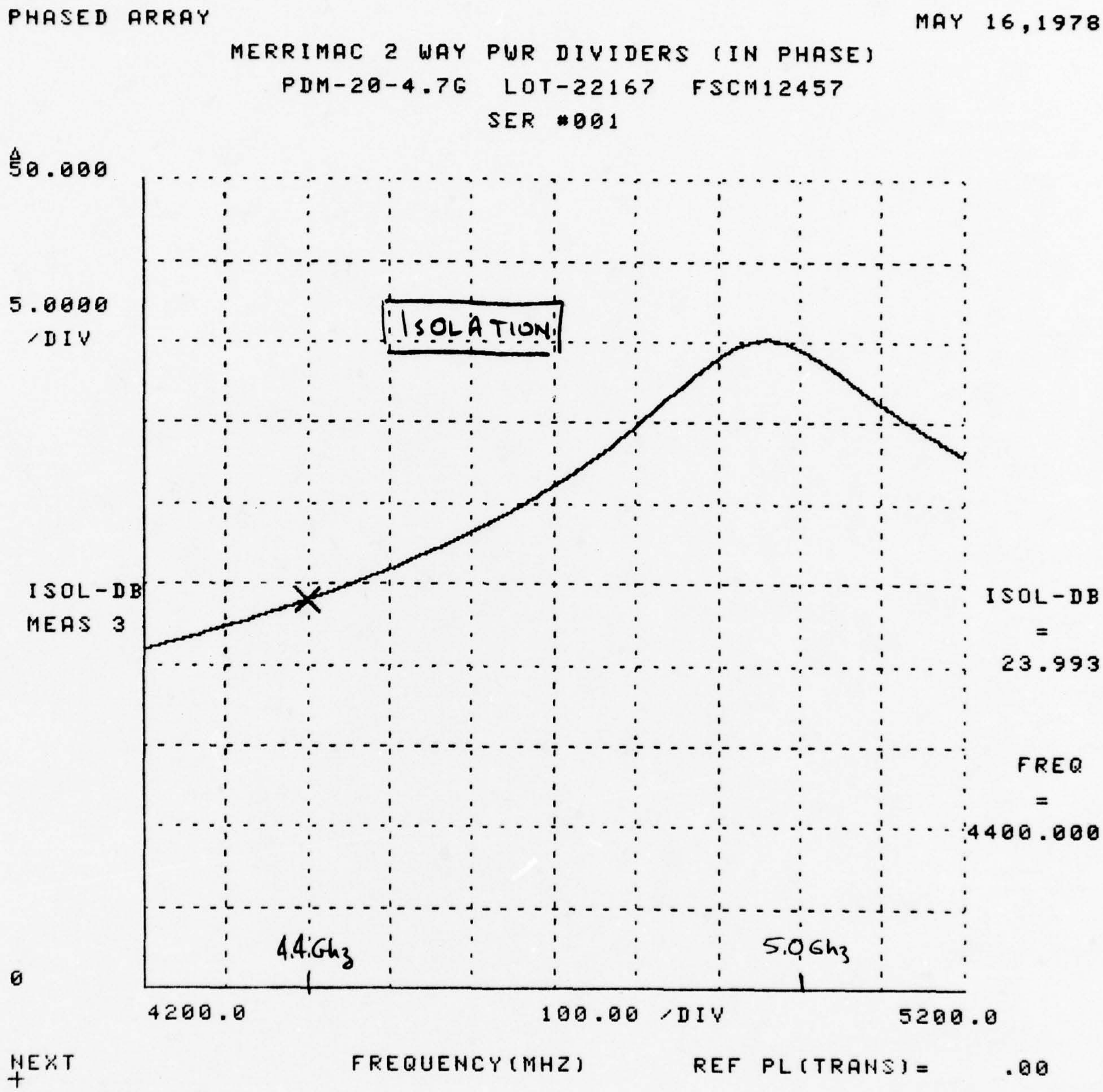


Fig 34



PHASED ARRAY
MAY 16,1978
MERRIMAC 2 WAY PWR DIVIDERS (IN PHASE)
PDM-20-4.7G LOT-22167 FSCM12457
SER #001
Δ
-5.000
1.0000
/DIV
Δ PHASE
PHASE
2 REL 1
PHASE
=
-1.184
FREQ
=
4700.000
4.4 Ghz
5.0 Ghz
5.0000
4200.0
100.00 /DIV
5200.0
NEXT
FREQUENCY(MHZ)
REF PL(TRANS)=
.00

FIG 35

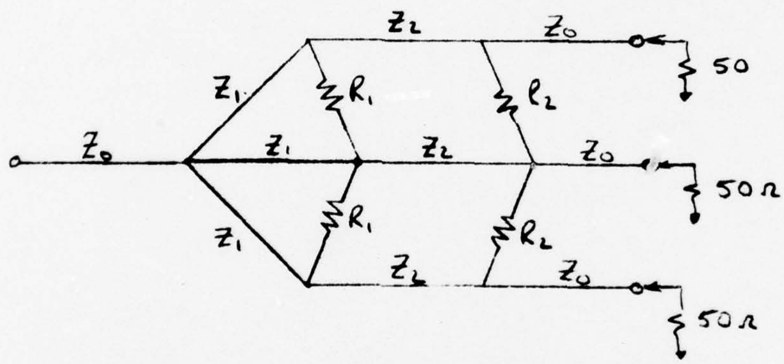


PHASED ARRAY
MAY 16,1978
MERRIMAC 2 WAY PWR DIVIDERS (IN PHASE)
PDM-20-4.7G LOT-22167 FSCM12457
SER #001
50.000
5.0000
/DIV
ISOLATION
ISOL-DB
MEAS 3
ISOL-DB
=
23.993
FREQ
=
4400.000
4.4Ghz
5.0Ghz
0
4200.0
100.00 /DIV
5200.0
NEXT
FREQUENCY(MHZ)
REF PL(TRANS)= .00

Fig 36

THREE WAY POWER DIVIDER

PLANAR WILKINSON



$Z_0 = 50\ \Omega$

$Z_1 = 114\ \Omega\ ,\ 90^\circ$

$Z_2 = 66\ \Omega,\ 90^\circ$

$R_1 = 65\ \Omega$

$R_2 = 200\ \Omega$

TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION		ANGLES	3 WAY PWR DIVIDER
	2 PLACE	3 PLACE		

USED ON	CODE IDENT. NO.	DWG.	PHASE ARRAY
PREPARED BY DATE	28528	A SIZE	
CHECKED BY DATE			SHEET FIG 37

DRAWING NUMBER

NUTLEY, NEW JERSEY

ITT DEFENSE COMMUNICATIONS DIVISION

D5215 A REV. 5/73

PHASED ARRAY 4/17/78

3 WAY DIVIDER

PRODUCTION UNIT

SER.3

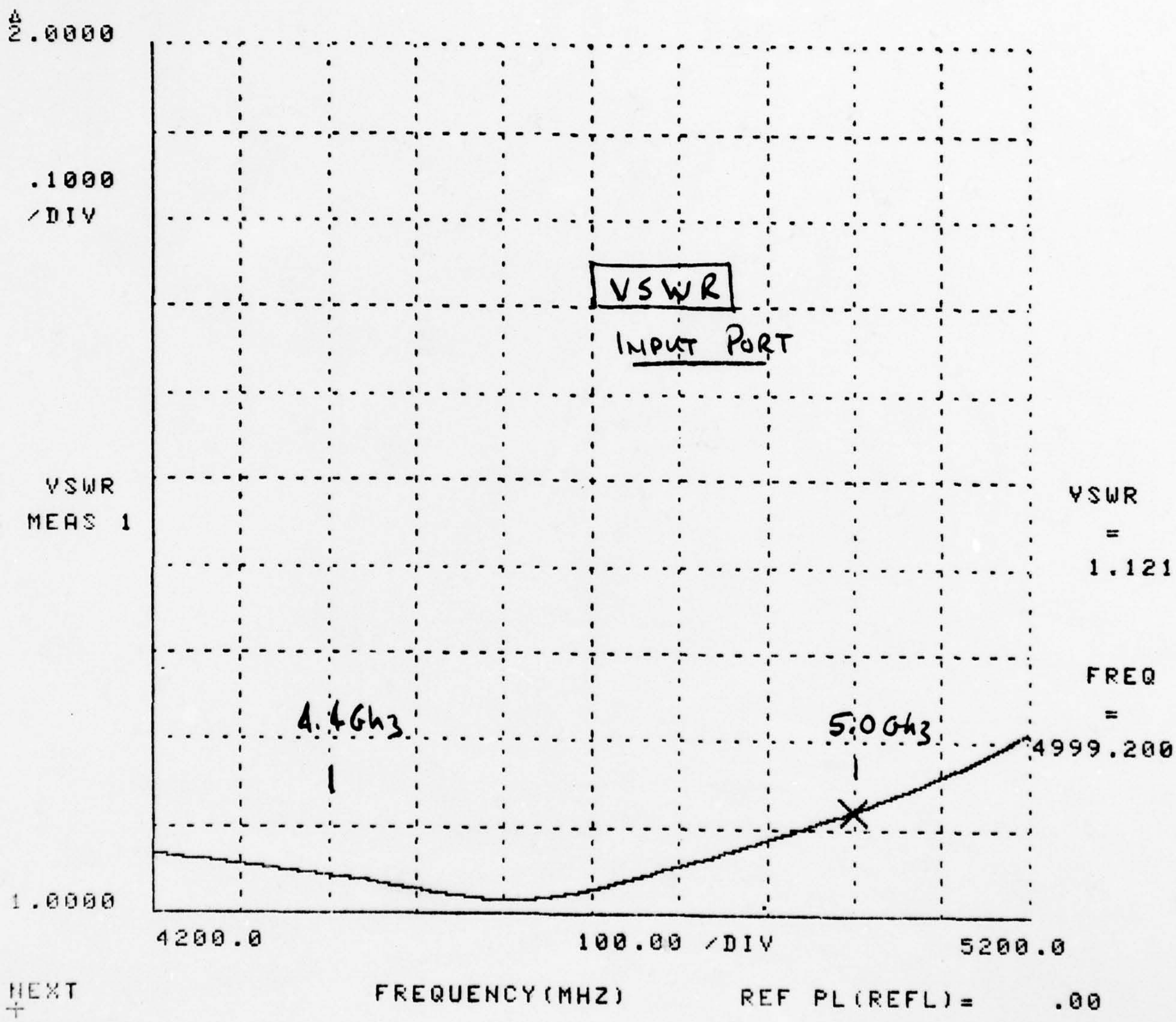


FIG 38

PHASED ARRAY 4/17/78

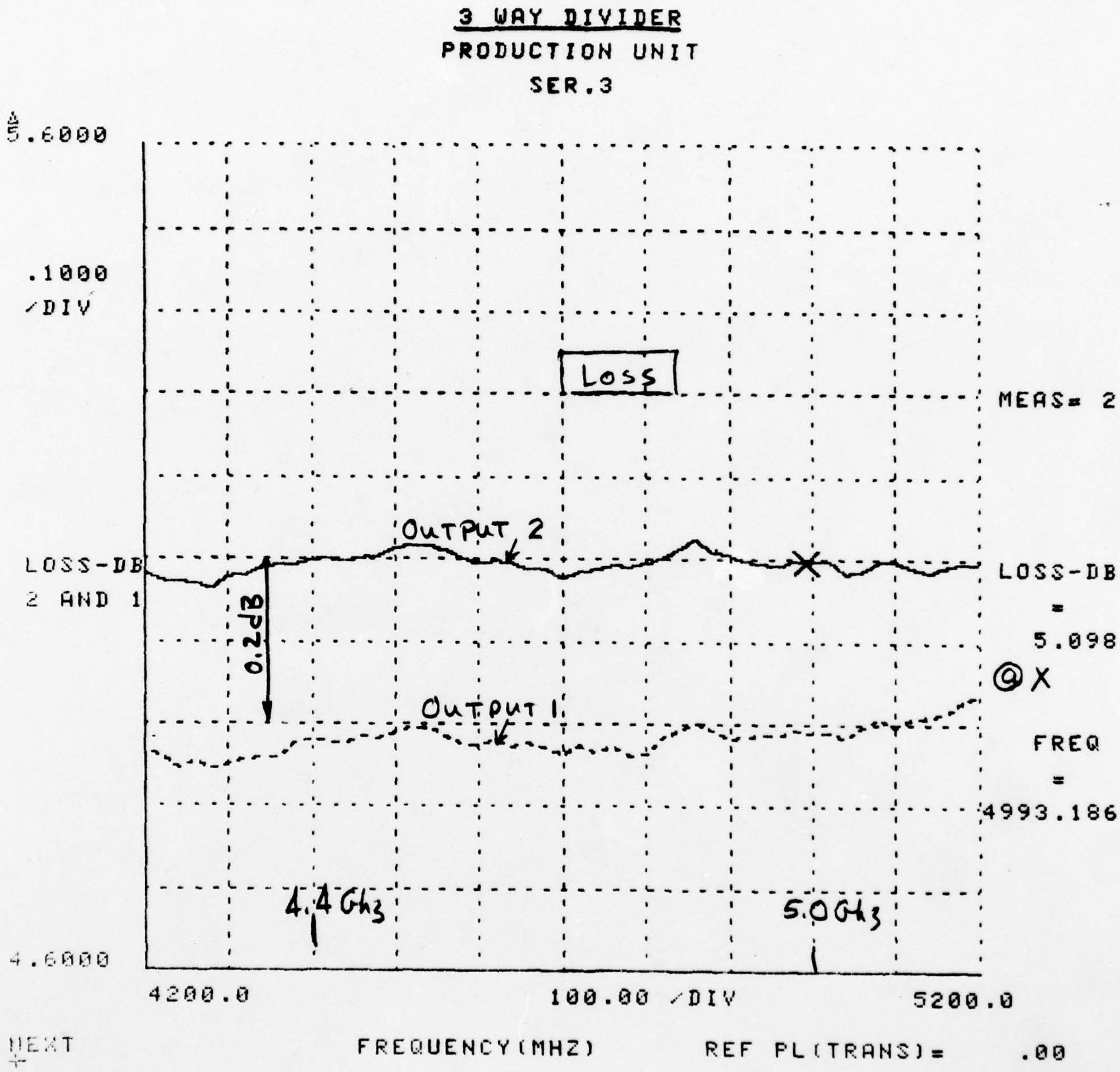
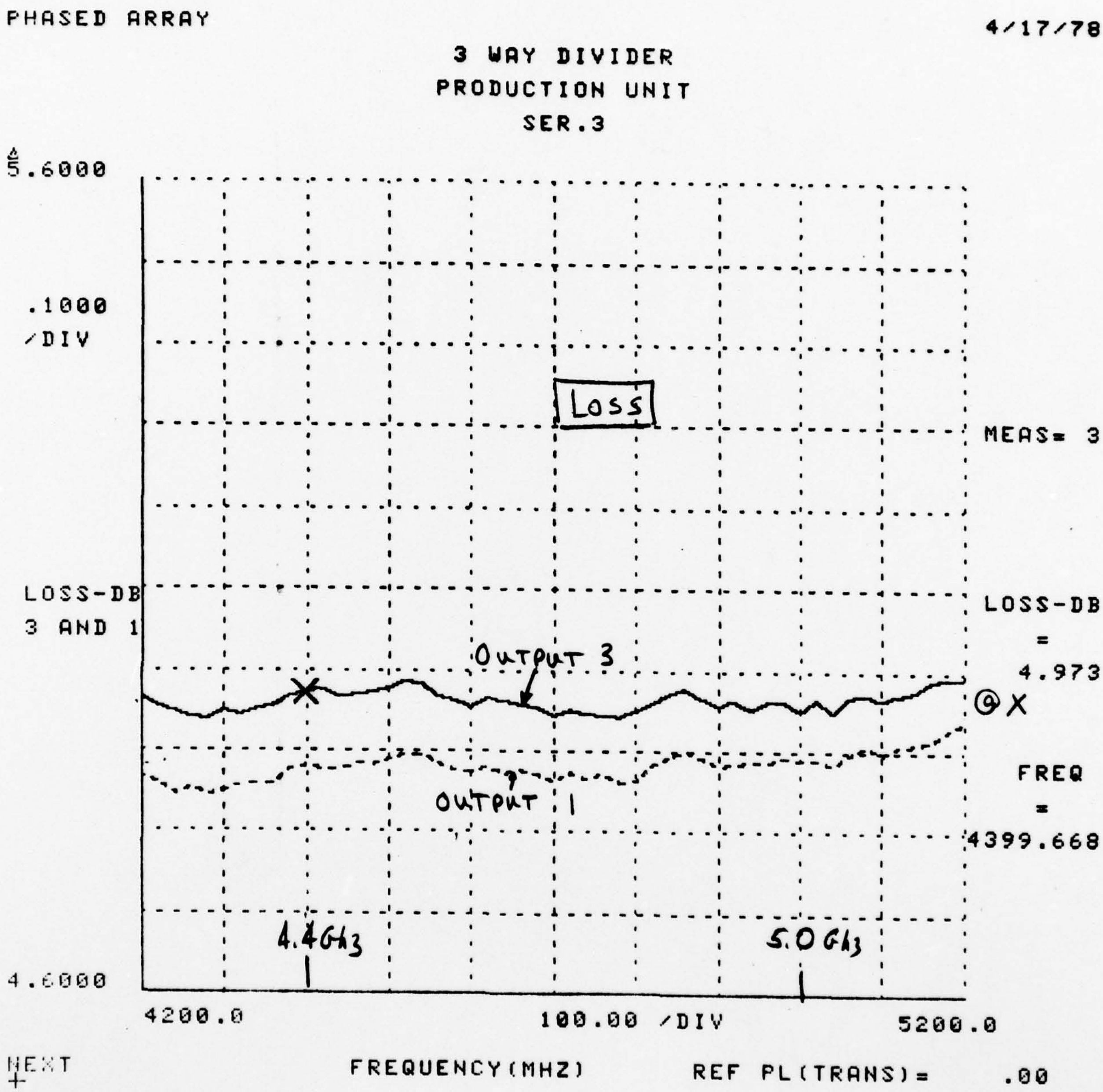


FIG 39



PHASED ARRAY
4/17/78
3 WAY DIVIDER
PRODUCTION UNIT
SER.3
5.6000
.1000
/DIV
Loss
MEAS= 3
LOSS-DB
3 AND 1
LOSS-DB
=
4.973
@X
Output 3
Output 1
FREQ
=
4399.668
4.4GHz
5.0GHz
4.6000
4200.0
100.00 /DIV
5200.0
NEXT
FREQUENCY(MHZ)
REF PL(TRANS)= .00

FIGURE 40

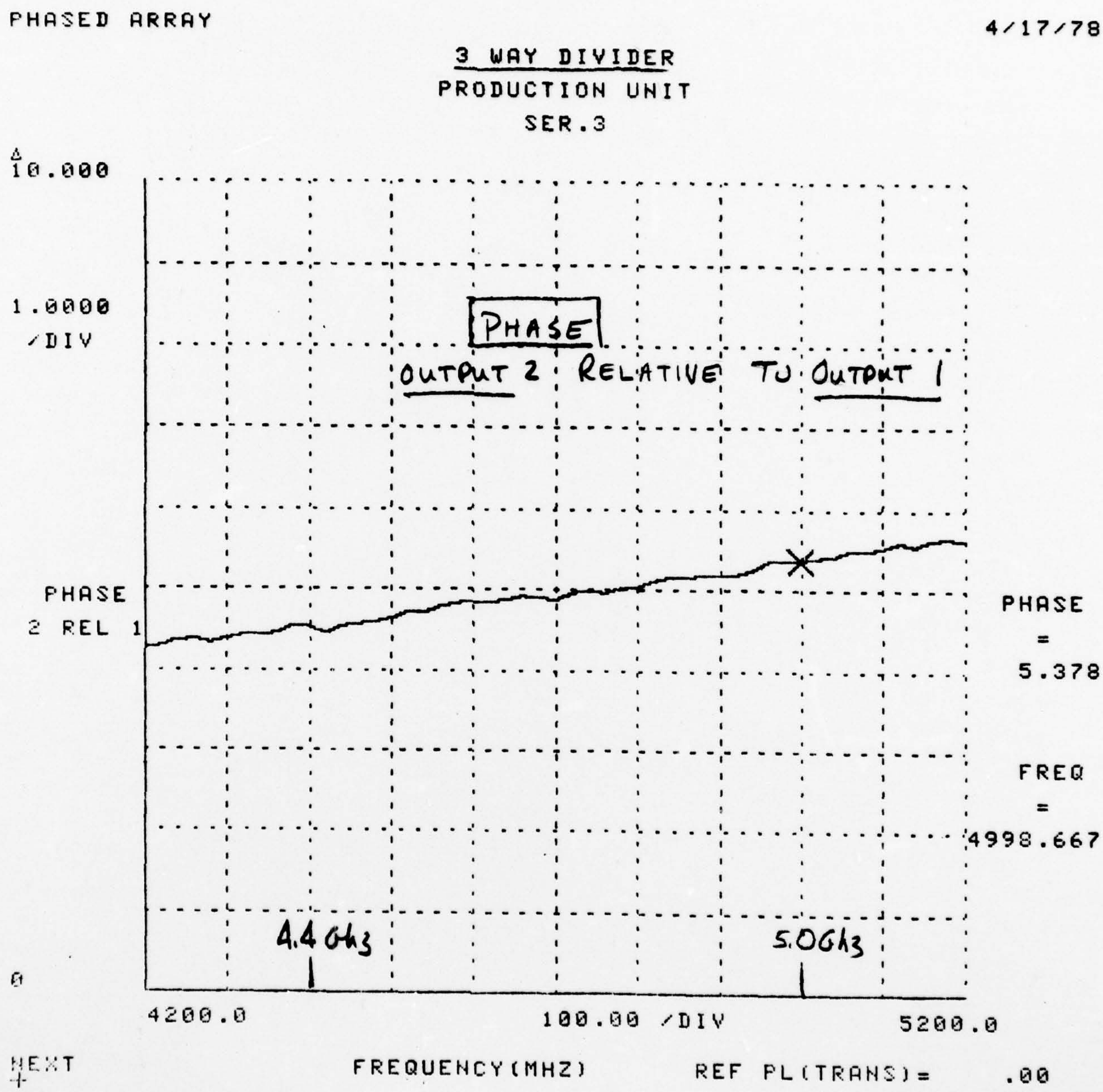

PHASED ARRAY
4/17/78
3 WAY DIVIDER
PRODUCTION UNIT
SER.3
10.000
1.0000
/DIV
PHASE
OUTPUT 2 RELATIVE TO OUTPUT 1
PHASE
2 REL 1
PHASE
=
5.378
FREQ
=
4998.667
4.4 Ghz
5.0Ghz
0
4200.0
100.00 /DIV
5200.0
NEXT
FREQUENCY(MHZ)
REF PL(TRANS)=
.00

FIGURE 41

PHASED ARRAY 4/17/78

3 WAY DIVIDER
PRODUCTION UNIT
SER.3

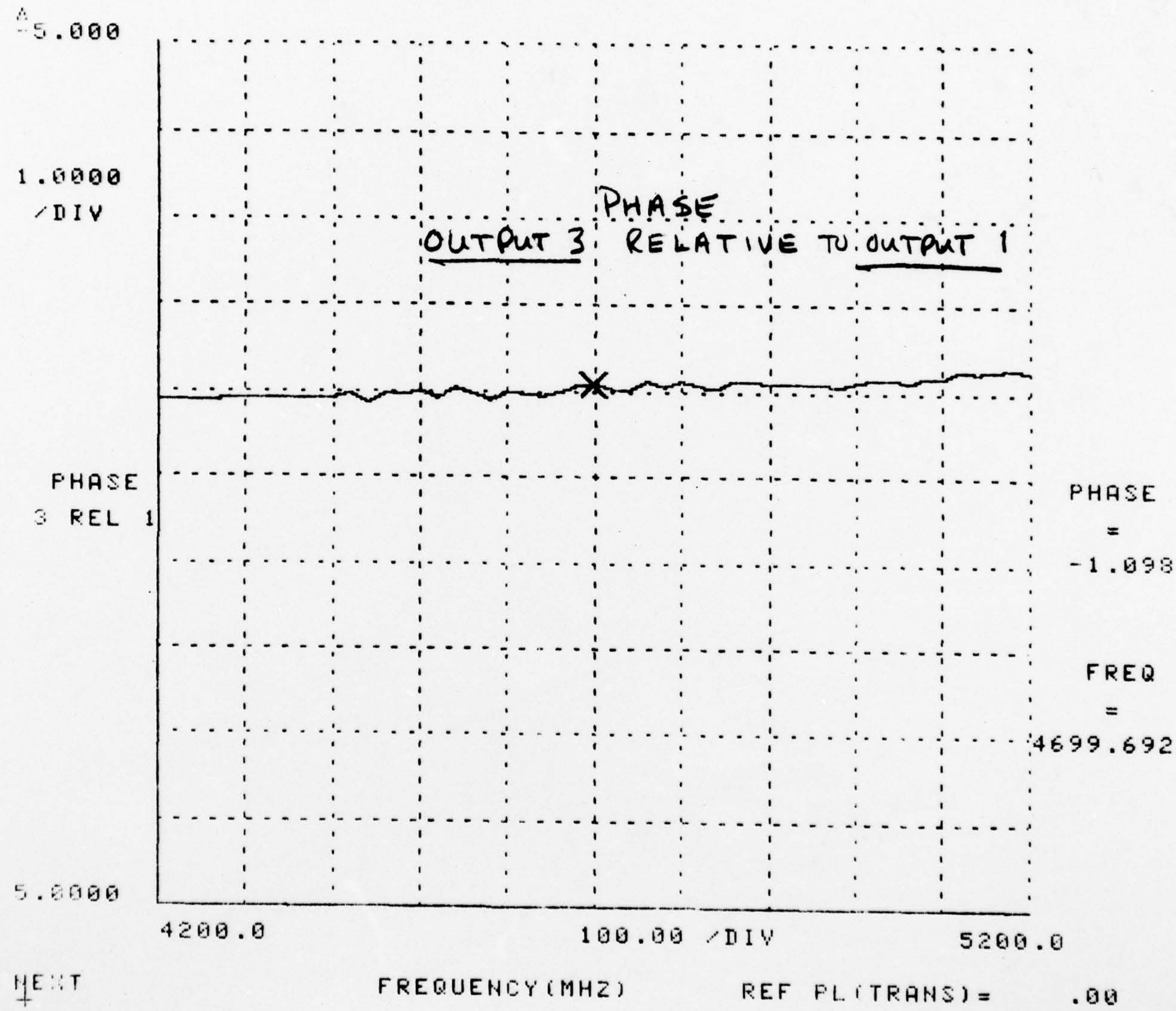


FIGURE 42

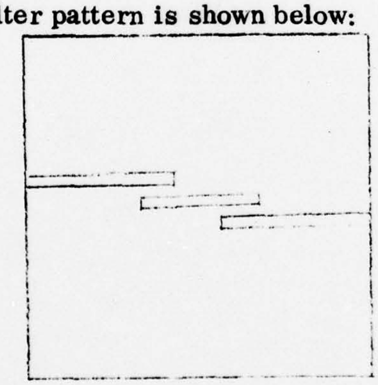
SUBSTRATE MATERIAL

Material Evaluation

Several substrate materials were investigated for use in the Phase Array amplifier modules. Besides alumina, ITT-DCD has studies less expensive materials such as Epsilam-10 (3M), teflon fiberglass, and fused quartz. Teflon fiberglass and fused quartz were unacceptable because their low dielectric constant made them incompatible with the 3 dB hybrids then being considered. Radiation at the inputs to these hybrids was minimal when launced into a material with a higher dielectric than used in the hybrid itself.

Since Epsilam-10 is less expensive than Alumina and, therefore, more attractive from a BPM cost viewpoint, an extensive comparison of the two materials was performed. The two differ mainly in loss tangent, thermal coefficient of expansion, and α_T (loss in dB/m). Their characteristics are outlined in Figure 43.

Two identical single resonator filters were constructed on the respective substrate material. The filter pattern is shown below:



SINGLE RESONATOR TEST FILTER

Both substrates were bonded to a carrier with end walls using the technique described in Section on Substrate Bonding.

FIGURE 43

ALUMINA AND EPSILAM-10 SPECIFICATIONS

PARAMETER	EPSILAM-10	ALUMINA
Dielectric Const. E_R	$10.2 \pm .5$	$10.1 \pm .25$
Temp. coeff. of E_R	570 ppm/°C	74 ppm/°C'
LOSS TAN δ (10 GHz)	.002	.0001
Metalization	Copper	Chrome-Gold
Thickness of metal	.00135"	.0003"
Coeff. of linear exp.	11-23 ppm/°C	7 ppm/°C
Loss/inch 4.7 GHz	.21 dB	.08 dB
Q_o at 4.7 GHz (50 Ω)	130	310
Cost/Sq inch	$1.00	$6.00

The filter was designed to resonate at 4.7 GHz, but actually resonated at 4.35 GHz due to fringing capacitance. It was felt that this shift in center frequency would not significantly effect the evaluation. All measurements were performed on an H.P. 8542B Automatic Network Analyzer. After an initial measurement was made, both filters were subjected to temperature and humidity extremes. After each environmental stress, the filters were retested at room temperature. The results of the evaluation are shown in Figure 44.

The loss in dB/inch can be expressed as:

$$T = \frac{27.3}{Qu\ \lambda_r}$$

Where λ_r is the effective wavelength in inches. The unloaded Q (Qu) is found by using graph T-99 of the 1963 Microwave Engineer's Handbook and Buyers Guide.

The results shown that Epsilam-10 is more lossy than Alumina due to a substantially lower Qu and its tendency to absorb moisture. This excess loss and undesireable tendency to alter characteristics via water absorption far outweigh its cost advantage. Based on these conclusions, Alumina was used as the substrate material.

Substrate Bonding

Previous programs at ITTDCD have extensively investigated the substrate/carrier interface. One major concern is the separation of the bond between these elements as a result of environmental factors. The standard technique employed at DCD has been Alumina epoxied to a Kovar carrier. This is reliable over environmental extremes, but increases weight and cost.

The Global Positioning Satellite (GPS) program at DCD had, as a prime consideration, weight. Thus, an investigation of reliable and lightweight substrate bonding

Condition	F_o (MHz)		VSWR		Loss (dB)		Loaded Q		Unloaded Q		α (dB/in.)	
	Alumina	E-10	Alumina	E-10	Alumina	E-10	Alumina	E-10	Alumina	E-10	Alumina	E-10
1) Initial Test	4350	4360	1.542	1.588	1.826	2.157	36.25	27.25	196.0	126.7	.14	.22
2) $50^{\circ}C$/ 4 Hours	4350	4370	1.54	1.627	1.792	2.132	36.42	27.14	199.6	127.4	.14	.22
3) $100^{\circ}C$/ 4 Hours		4370		1.381		2.115		27.48		129.6		.21
4) $0^{\circ}C$/ 4 Hours	4350	4350	1.473	1.548	1.860	2.495	38.16	27.53	200.8	112.4	.14	.25
5) H_20/soak 72 Hours	4350	4190	1.422	1.674	2.006	3.936	36.55	23.54	180.9	64.5	.15	.43
6) $100^{\circ}C$/ 4 Hours	4350	4390	1.517	1.453	1.912	2.185	36.86	27.10	191.0	124.3	.15	.22

FIGURE 44

ALUMINA VS EPSILAM-10

TEST RESULTS

techniques ensued. The results of this analysis led to a technique of bonding Alumina to Aluminum via conductive epoxy. This technique was subjected to repeated thermal cycles (> 40) without separation.

For the Phased Array Antenna Amplifier Program this technique has allowed DCD to reduce the weight of a basic power module by approximately .5 pounds. This is based upon .28 lb/cu. in. for Kovar and approximately 6 sq. in. of carrier per BPM. Additionally, the expense of machining Kovar has been eliminated.

II G. SUMMARY & RECOMMENDATIONS

The Exploratory Development Scale Model of the (mechanically steerable) Phased Array Antenna Amplifier has demonstrated the feasibility of solid state power generation and spatial combining for communication system applications. Though not every specification was met, the major factors affecting system performance were detailed and demonstrated.

SUMMARY

The success of this program exists in the analysis, design, and test of new microwave components in a dual diversity communications system. These areas are:

- Printed Circuit Dual Polarized Array
- Computer Aided Design (CAD) Accomplishments in Array Antenna Design
- High Efficiency Broadband RF Amplifiers
- Duplex Operation of a scale model system employing distributed RF power generation (graceful degradation) and spatial combining.

PRINTED CIRCUIT DUAL POLARIZED ARRAY ACCOMPLISHMENTS

The major accomplishment of the antenna design was to realize in simple hardware a complex system requirement. The complexity included:

- Multiple inputs
- Greater than 1000 radiating elements
- Sub-array combining corporate feeds
- Dual independent polarizations
- Electrical performance comparable to a standard parabolic reflector antenna
- Single aperture with normal gain/area antenna performance for dual polarizations
- Readily extendable to other sizes.

The solution to meet these requirements was a simple arrangement of three printed circuit laminates layered above a flat ground plane and with coaxial input/output connections to sub-arrays, a structure capable of further simplification to a single laminate and ground plane.

Realization of the antenna required new technology advances in designing and fabricating large single piece PCB laminates as well as advances in modelling of physical parameters to meet electrical performance requirements. The latter is especially important because of the great cost of artwork development for large laminates. Thus, ten square foot apertures of a single piece have been demonstrated as <u>feasible</u> in construction and <u>predictable</u> in performance.

The electrical performance, as measured and by extrapolation with feasible design improvements, demonstrated that the increase in complexity did not result in sub-par performance with respect to the standard field parabolic antenna. Thus, 50 to 55% efficiencies were achieved and 60% appears feasible. Beamwidth and sidelobes were shown to be capable of adjustment by aperture shape and taper to

within tenths of a degree for beamwidth and 1 to 1.5 dB for sidelobes. VSWR performance of 1.5:1 maximum, attainable in a fully optimized design, is compatible with system needs although higher than typical parabolic-feedhorn VSWR. Finally, isolation performance of 30 dB minimum between polarizations and greater than 40 dB between sub-arrays within a polarization demonstrate the array techniques are comparable to typical parabola-horn antennas without degradation due to blockage.

In addition to the contract application, the use and attainment of sub-array, mutli-port construction for both transmit and receive provides a tool for other applications by array processing techniques. Some possibilities are:

- Receive array null steering for tracking or anti-jamming
- Receive and/or transmit rejection of unwanted frequencies by array processing of sub-arrays as a filter
- Simultaneous operation on different frequencies (equal to the number of sub-arrays) for transmit and /or receive, i.e., a multi-beam antenna
- Noise and fade cancellation by sub-array processing
- Special modulation techniques
- Polarization diversity.

The array is a versatile vehicle which provides a minimum of hardware complexity in implementing complex system functions.

CAD ACCOMPLISHMENTS IN ARRAY ANTENNA DESIGN

Large printed circuit arrays pose special problems in design and fabrication which make it mandatory to have a method for accurately predicting performance. Computer Aided Design (CAD) provides the needed computational power to directly assess the performance of large arrays with arbitrary excitations not amenable to closed form solutions. Thus, the successful use of CAD techniques is in itself a program achievement.

Three areas of investigation resulted from the three main causes of variations in aperture excitation: applied tapering for sidelobe control, errors due to tolerances of construction and input powers, graceful degradation performance due to total loss of one or more input signals. Achievements in each of these areas by CAD were as follows:

	CAD	Measured
• <u>Taper Selection</u>:		
Sidelobes, cardinal	17.0 dB	16.3 dB (Avg)
inter-card.	21.0 dB	20.1 dB (Avg)
• <u>Error Performance:</u>		
(Fabrication & excitation errors)		
Sidelobe degradation - Avg.	1.9 dB	0.7 dB
Peak	3.5 dB	2.9 dB
Gain error - Tx	.54 dB	1.05 dB
Rx	.54 dB	1.34 dB
• <u>ERP Degradation:</u>		
Single Amplifier failure	1.43 dB (Avg)	1.7 dB (Avg)

From these results, the CAD analysis was quite accurate in predicting actual averaged performance. It is expected that expanding this CAD to larger arrays would provide very useful information in determining -

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PHASED ARRAY ANTENNA AMPLIFIER EXPLORATORY DEVELOPMENT MODEL.(U)

AUG 79 P MUSCIANESI, J IRVINE, J RANGHELLI DAAB07-77-C-0146

UNCLASSIFIED CORADCOM-77-0146-F NL

2 OF 4

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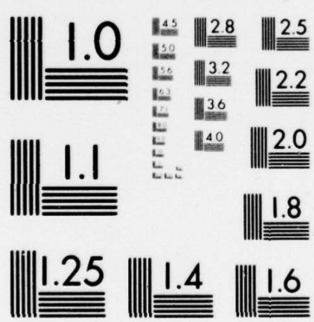


MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

- Feasibility of printed array - spatial combining technique for further extensions of this system and for new concepts.
- Design characteristics for achieving the desired results.

During the course of this program, both Silicon Bipolar Transistors and Gallium Arsenide Field Effect Transistors were considered for use in the amplifiers. In addition to these two device technologies, ITT also investigated the various design techniques for power combining/splitting to efficiently add the power of individual devices to form higher level signals.

In all cases the main consideration was to develop the technology required to demonstrate system feasibility.

As a result of this driving consideration, when it became apparent that current high power Bipolar devices offered severe drawbacks to system performance, ITT developed the Gallium Arsenide FET Amplifier. As a result of this evaluation effort, ITT was able to provide a side by side comparison of the devices' performance. Following is a general summary of this comparison (Refer to Extended Amplifier Tests - for specifics Appendix B).

> NOTE: This comparison is valid with current components; levels, limits, etc. will change as progress is made in each technology.

This evaluation (comparison) listed those device parameters most critical to Duplex communications system performance.

Parameter	Silicon Bipolar	Gallium Arsenide FET
Bandwidth	300 MHz (Partial Band)	600 MHz Minimum (Full Band)
Drive Sensitivity	Non-Linear, bandwidth critically dependent upon drive Class 'C' bias	Linear, bandwidth insensitive to drive Class 'A' bias
Power Output/Device	4.5 Watt	2.5 Watt
Device Efficiency	23% @ Nominal Drive	28% @ Nominal Drive
Amplifier Efficiency	16% Measured	22% Measured
DC Power Source	Positive (+26 v)	Positive (Drain) (+8.5 volt) Negative (Source) (-2 volt)
Noise Power	-136.5 dBm/Hz	-144.9 dBm/Hz
Noise Figure Degradation (AN/GRC-143 Receiver & Scale Model System)	3 - 4 dB (Calculated)	None (Measured)
Second Harmonic	-28 dBc	-38 dBc
AM/PM Conversion	10^{o} dB	3^{o}/dB
Phase Tracking	23^{o}, transistor to transistor	46^{o}, BPM to BPM (2 BPM's within 15^{o}, one within 46^{o})
3rd Order Intercept Point	-	+45.6 dBm
Device Package	Epoxy Seal	Hermetic
Metalization System	Gold	Gold

Duplex Operation

For this exploratory development effort to be considered successful, one of the most critical system characteristic which had to be demonstrated was Duplex Operation. This characteristic was demonstrated by both calculating and measuring the effects of the Phased Arrays' Transmit Chain and cross polarization coupling on an AN/GRC-143 Receiver.

The details of these effects are outlined in the Test Plan Data, Appendix A of this report.

The results show that no measureable difference occurs in the AN/GRC-143 Receiver Threshold with the Phased Arrays' Transmitter (GaAsFET Design) on or off for Receive and Transmit frequencies separated by 100 MHz. This was repeated at more than one frequency setting with similar results.

The GaAsFET amplifier noise power output 100 MHz away from the carrier was measured to be -145 dBm / Hz. This was approximately 8.4 dB below the noise power measured for the TRW MRA 271 bipolar transistor. Noise quieting curves for the AN/GRC-143 Receiver with and without the Phased Array Antenna Amplifier showed no degradation in receiver threshold with 100 MHz transmit to receive frequency separation. This is the minimum frequency separation normally used and thus full duplex operation of the AN/GRC-143 is possible with this Phased Array Antenna Amplifier system.

At 50 MHz separation (less than required for system operation), a 4 dB degradation in receiver threshold was measured. This equates to a 4 dB receiver noise figure degradation. From figure 45 it is estimated that the FET amplifier noise power 50 MHz away from the carrier is -137 dBm / Hz, or just about the same noise power output measured from the bipolar transistor 100 MHz away from the carrier.

Δ

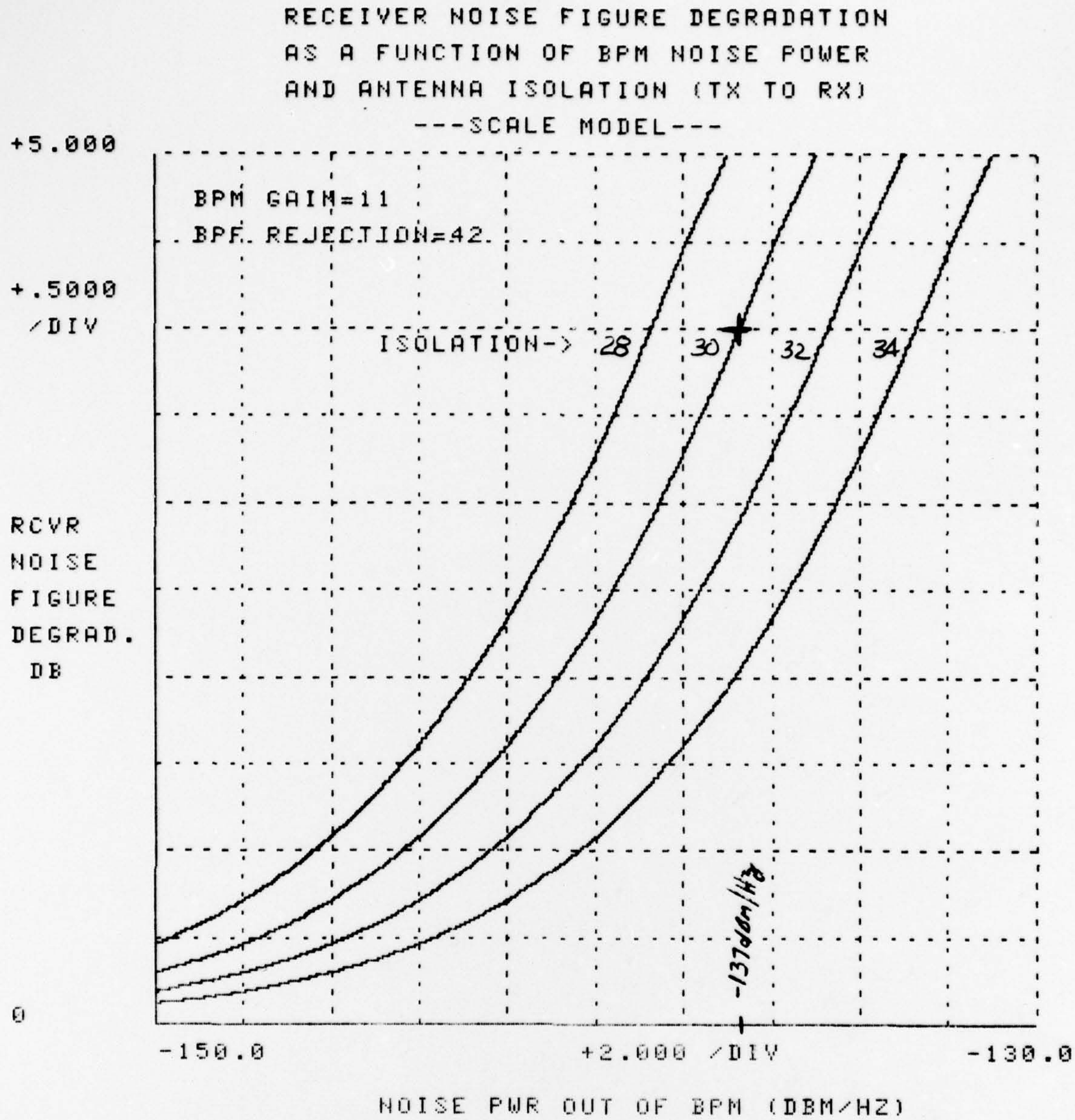

RECEIVER NOISE FIGURE DEGRADATION
AS A FUNCTION OF BPM NOISE POWER
AND ANTENNA ISOLATION (TX TO RX)
---SCALE MODEL---
+5.000
+.5000
/DIV
BPM GAIN=11
BPF REJECTION=42
ISOLATION-> 28 30 32 34
RCVR
NOISE
FIGURE
DEGRAD.
DB
0
-150.0
+2.000 /DIV
-130.0
NOISE PWR OUT OF BPM (DBM/HZ)
-137dbm/Hz

FIGURE 45

Thus it has been demonstrated that full duplex operation of the AN/GRC-143 is possible with the Phased Array Antenna Amplifier. The key technical developments that were required to achieve this goal were:

- High transmit to receive polarization isolation (30 dB minimum, > 35 dB typical)
- Low noise power output from the GaAsFET power amplifiers (-145 dBm / Hz @ 100 MHz from carrier)
- System design with proper gain in antenna mounted BPM's and Bandpass filter rejection to reduce IPA noise contributions.

RECOMMENDATIONS

In order to successfully extend the Scale Model Exploratory Development effort to a full scale IKW Program, development work in several areas is required. These areas are:

- Low Loss, Light Weight RF Power Distribution Techniques
- Development of a Dual Polarized Printed Dipole Antenna on a single Laminate
- Extension of CAD (Computer Aided Design) to predict Antenna Performance for various Amplitude tapers.
- High Power Transistor Technology in the 4.4 - 5.0 GHZ Band.
- Low Loss, Light Weight, Inexpensive substrate material for Microwave Integrated Circuits.

RF POWER DISTRIBUTION

The scale model antenna used .141 inch diameter semi-rigid coaxial cable to integrate the receive sub-arrays and also for power division to the amplifiers. Due to the buffering effect of the amplifiers the cable losses do not significantly affect transmit gain but the losses directly reduce receive gain. by 1 to 1.5 dB. The extension to a full scale antenna would increase this loss prohibitively unless a low loss transmission is used. Section III C discusses trade-offs which show the desireability of using a waveguide structure. Although mandatory for receive, waveguide has advantages for transmit and consequently a parallel system is proposed.

A development program to realize a low loss distribution system would provide a key element in realizing an efficient antenna. Areas to be developed are:

- dual mode versus stacked single mode guides.
- dual mode wave guide components - power dividers, bends, coax transitions
- low weight techniques
- mechanical integration into antenna structure

SINGLE LAMINATE ANTENNA

A major source of weight, cost and complexity in the antenna is the requirement for three super-imposed printed circuit laminates to achieve dual polarization for independent transmit and receive. The possibility of a dual polarized single laminate antenna was rejected as a risk approach in the initial scale model analysis, section II F. Subsequent refinement of the concept has shown a viable realization is possible which was used as the basis for the IKW model, section III C.

A development program to reduce the single laminate concept to a practical design applicable to the IKW antenna would provide a basic building block for the antenna realization. The goals to be attained are:

- layout and artwork development of an 8 x 8 array of two independent orthogonal dipole arrays with their corporate feeds, and useable for developing final sub-arrays of the IKW antenna by step and repeat photography.
- optimization of VSWR performance by broadband dipole matching techniques.
- determination of isolation between polarizations
- optimization of geometry to minimize spurious radiation for improved side lobe control

COMPUTER AIDED DESIGN

The increase in the number of dipoles for the IKW antenna as compared to the scale model overextends the PDP-11 computer system for which the scale model computer program was written. A reduction technique was used to develop the IKW system which grouped small sub-arrays of equal power in order to reduce the array size. Whereas this is satisfactory for nominal tapers, it is not useable for analysis of errors distributed throughout the array, i.e., with errors, the grouped dipoles are no longer of equal voltage. In addition, the interlacing scheme for a single laminate design, as well as the modular construction of the antenna will result in new type error patterns associated with sub-array boundaries. Thus, a revision of the computer aided design program to accomodate the larger array and the new error models is recommended. The needed increase in computer power is available in a recently acquired IBM 370 computer.

An additional task recommended for an improved computer program is the modeling of spurious radition from the feed lines as part of aperture excitation. This would provide data for predicting and controlling of spurious sidelobes

High Power Transistor Technology

The proposed 1 Kw is based upon transistor performance that is currently not available in production quantities. The transistor performance required is summarized below.

	Driver Stage	Power Stage
POUT	17.4 watt	3.2 watt
Gain	7.5 dB	8.4 dB
Efficiency	35%	35%
V_{DS}	20 volts	20 volts

These specifications are not too far from the results recently reported at the 1979 International Microwave Symposium by K. Honjo, etal of Nippon Electric Co. They reported on an internally matched GaAsFET capable of 12.6 watts output power with 5 dB gain (6.5 dB small signal) and 30% power added efficiency at 6 GHz. Continued progress in high power GaAsFET's is certainly forthcoming as the material processing, device characteristics and matching techniques improve. Section III B will detail the required device parameters for the proposed 1 Kw system.

Substrate Material for Microwave Integrated Circuits

The substrate material used in the scale model Basic Power Modules is Alumina. For a 1 kw system, the much larger number of substrates required ($\sim$150/system) would certainly justify an investigation to identify lower cost alternate materials. Several high dielectric materials ($Er \simeq 10$) are presently being manufactured which offer significant cost savings over alumina. An evaluation similar to the one conducted with 3M's Epsilam-10 would have to be performed to evaluate their usefulness in the 1 kw BPM's. These materials (Rogers Corp RT/Duroid 6010 and Keene Diclad 810) appear to offer at least a 5:1 cost advantage over Alumina. These materials can be purchased with 1/3 or 1/4 oz copper plating (instead of the normal 1 oz) making fabrication of Lange couplers possible. Any investigation of these materials should include etching very narrow line widths and gaps such as would be required in a Lange coupler.

III A. SYSTEM DESIGN

1 KW Phased Array Antenna Amplifier

The purpose of this section is to detail a system approach for a 1 KW Phased Array Antenna Amplifier. This system concept is based upon the results obtained with the Scale Model Phased Array system. For the purpose of developing this system, the following preliminary specifications have been assumed.

Frequency		4.4 - 5.0 GHz
RF Power Output		1 KW (Min)
Efficiency	DC - RF	20% (Min)
	AC - RF	15% (Min)
Antenna Gain		40 dBi
Sidelobes		-18 dB
Beamwidth		1.5°
ERP		+100 dBm
Antenna Weight		500 lb. (max)
Duplex Operation		$\leq$ 1.5 dB Receiver N. F. Degradation
Set-Up Time		1 hour
MTBF		4000 hours prior to 3 dB loss in ERP
Control Circuity and Power Supplies		Weight: Size: Present AN/GRC-143 (AM-6090) 1 kw Klystron HPA

The output of this effort will include a system block diagram, a detailed antenna approach and the transistor performance required to meet the system specifications. This will include transistor output power, gain, efficiency, and MTBF requirements.

System Design

The development of the system concept involved a number of tradeoff areas which were investigated. In all cases, the basic concept was that of the Scale Model system; that is, a control cabinet containing an IPA and an antenna mounted RF distribution network with a number of amplifier modules. Tradeoff areas that were investigated included:

1. Number of Antenna Basic Power Modules (BPM's)

The tradeoff here is whether to use many low power amplifier modules or fewer high power modules. Favoring the low power amplifier approach are thermal, transistor capability, and system graceful degradation considerations. The disadvantages of this approach include the additional complexity, loss in the RF power distribution network and cost of many BPM's.

2. Gain of the Antenna BPM's

The RF gain of the antenna mounted BPM's must be optimized in terms of its impact on receiver noise figure degradation and on the output power required from the IPA. Low gain modules minimize the transmitter noise power presented to the receiver but require additional power from the IPA to make up for the low gain. Additional parameters such as system efficiency and reliability must also be considered.

3. Technique to Obtain Antenna Taper

Several techniques for deriving the antenna taper were considered. These include:

- Equal power amplifiers driving unequal number of dipoles. This is the method used in the Scale Model Antenna but is not considered feasible for a full size antenna due to cost and field deployment considerations.
- Unequal power amplifiers driving equal number of dipoles. This approach greatly eases the antenna but requires solution to the problem of controlling transmission phase of different power transistors or even the same transistors at different power level/biasing conditions.
- Equal Power Amplifiers, some followed by power dividers. This method requires that the transmission phase of the different power dividers be compensated for with various lengths of transmission line.

The method selected is a modification of the last technique with all paths have the same number of power dividers and hence the same electrical length.

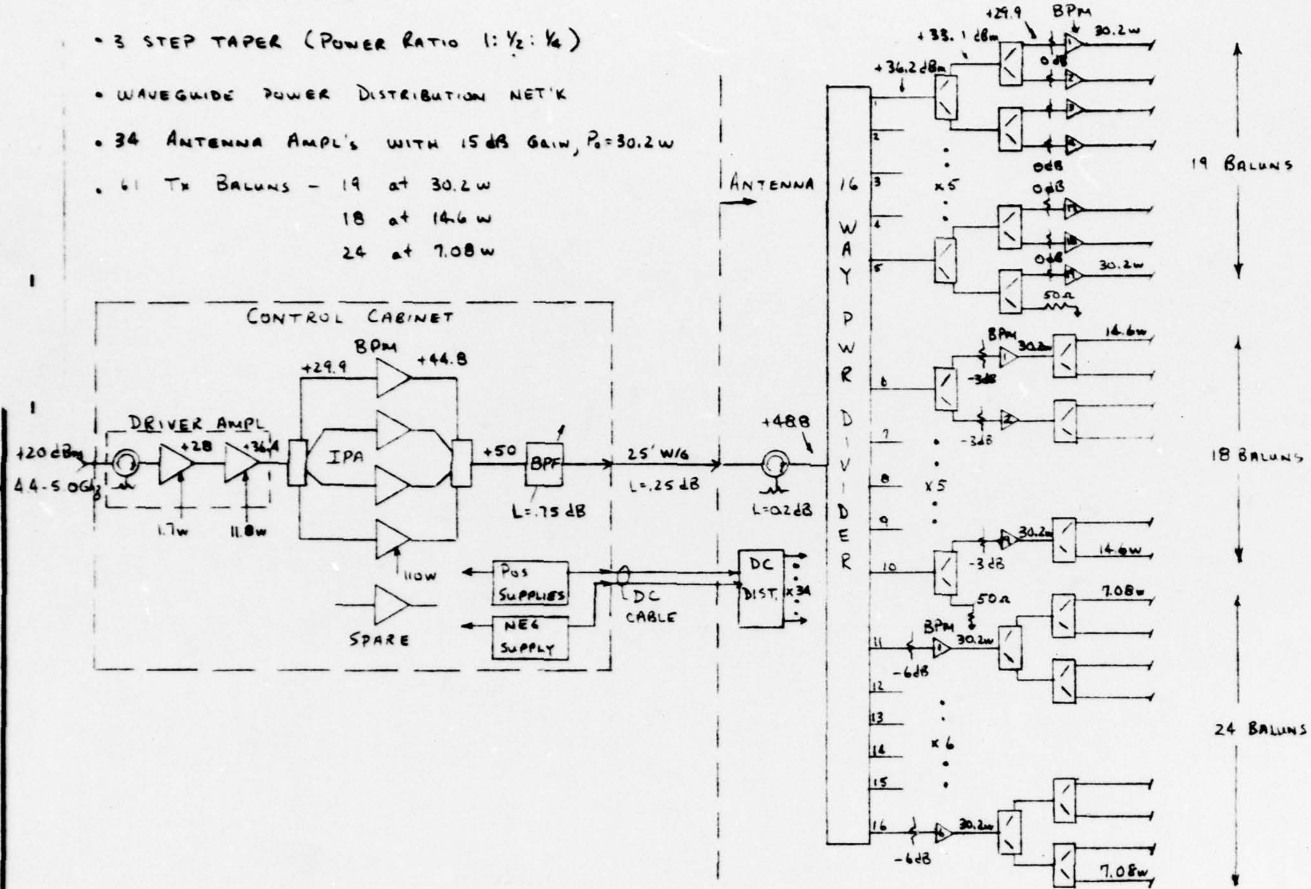
The block diagram for the 1 KW Phase Array Antenna Amplifier system is shown in Figure 45. The system consists of a Control Cabinet containing an IPA module which is made up of four BPM's, a driver amplifier and all the power supplies required for the system. A BPF follows the IPA. The BPF is required to reduce IPA noise power 100 MHz away from the carrier frequency.

A 25 foot waveguide run is proposed for this system since the limited flexibility of the 7/8 inch diameter Heliax cable used in the Scale Model does not justify its higher loss (typically 1 dB). This waveguide run would include enough flexible sections to enable antenna positioning.

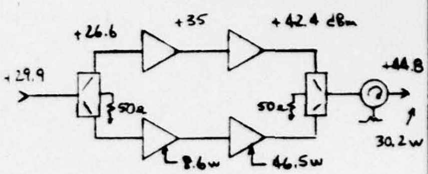
The antenna RF distribution network would be realized in waveguide, possibly dual mode, to minimize the RF losses associated with the lengths of transmission line required to cover the full scale antenna. The amplifiers are equal power units, each capable of 30 watts output power, which are distributed <u>within</u> the waveguide network. All power dividers shown would be low loss waveguide designs. The 16 way power divider shown consists of fifteen in phase, 3 dB hybrids distributed around the array. The amplifier block would include a W/G to coax transition, a short length of coax cable (possibly low loss flexible), the amplifier itself and for some modules, a second W/G to coax transition to get back into the RF distributor network. The antenna taper is achieved by driving the transmit baluns either directly from a BPM, from a BPM followed by a waveguide 3 dB hybrid or from a BPM followed by two 3 dB hybrids. This provides the desired antenna taper of 1:1/2:1/4 power ratio. Note that each path from antenna input to transmit balun has the same number of 3 dB hybrids. This is accomplished by placing the various BPM's within the RF distributor network. To avoid the situation of driving amplifiers at different RF levels, 3 dB or 6 dB attenuators would be included as shown in the block diagram. The 19 amplifiers that directly drive baluns would include a 0 dB attenuator with the same phase characteristics as the 3 dB and 6 dB attenuators. These attenuators could be either waveguide or coax. The loss of system efficiency from these attenuators is minor considerating the advantage of equal power, equal gain amplifiers that is obtained.

1 KW SYSTEM

- 3 STEP TAPER (POWER RATIO 1: 1/2 : 1/4)
- WAVEGUIDE POWER DISTRIBUTION NET'K
- 34 ANTENNA AMPL'S WITH 15 dB GAIN, $P_o = 30.2\,w$
- 61 Tx BALUNS – 19 at 30.2 w
  18 at 14.6 w
  24 at 7.08 w



BASIC POWER MODULE



$P_o = 30.2$ watt

$P_{DC} = 110$ watt (20v @ 5.51 amp)

Eff = 27.4% (ASSUMING 35% TRANSISTOR EFFICIENCY)

SYSTEM

$P_o = 19(30.2) + 18(14.6) + 24(7.08)\,w$

$P_o = 1006$ WATTS

$P_{DC} = 34(110w) + 4(110w) + 11.8 + 1.7\,w$

$P_{DC} = 4193$ WATTS

$EFF = \frac{P_o}{P_{DC}} \times 100\%$

EFF = 24.0%

FIGURE 45

TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL-DIMENSION 2 PLACE	3 PLACE	ANGLES	DRAWN BY / DATE	CHECKED BY / DATE	APPROVED BY / DATE	ITT DEFENSE COMMUNICATIONS DIVISION	NUTLEY, NEW JERSEY	SIZE B	CODE IDENT. NO. 28528	1 KW PHASED ARRAY
									SCALE	REV.	SHEET 103

D6216 B REV. 6/73

ANTENNA

The antenna is a 3 step (1: 1/2: 1/4) design which provides 40 dBi gain with sidelobes at least 20 dB below the main beam. Extensive computer simulation was performed to obtain this quasi-circular operation design which achieves high gain while maintaining minimum sidelobes in all directions. The antenna is dual polarization printed on a single laminate. This represents a major change from the 3 laminate approach utilized on the Scale Model and would require development but offers significant weight, set-up time as well as probable electrical advantages. These are discussed in more detail in the antenna section. The antenna consists of 61 sections (sub-arrays) each with a transmit and receive balun which interfaces with the transmit and receive RF distribution network. The receive network would be identical to the transmit with the taper being obtained with 0, 3, and 6 dB attenuators but the amplifier modules. Dual modes waveguide would be seriously considered so that a single distribution network would provide both transmit and receive functions. Several problems such as the realization of dual mode power dividers would have to be resolved before this approach could be implemented. Alternatives such as reduced height waveguides are possible work-arounds and are discussed in more detail in the section on antenna tradeoffs. Figure 46 illustrates the concept proposed for the antenna. The antenna consists of three "rings" corresponding to the 3 step taper. The inner consists of 19 antenna sub-arrays each with a balun directly driven by a BPM. The center "ring" consists of 18 subarrays driven from 9 BPM's followed by a 3 dB hybrids providing the power taper factor of 1/2. The outer "ring" consists of 24 sub-arrays driven from 6 BPM's followed by 2 - 3 dB hybrids providing the power taper factor of 1/4. The layout shows approximate amplifier placement along with the RF routing required to achieve equal line lengths for all baluns phasing.

Graceful Degradation - Using a loss of 3 dB in ERP as the definition for a system failure, the number of BPM's that could fail without loosing 3 dB in ERP was investigated. Contributions from both loss of power and antenna gain were evaluated as a function of amplifier failure and amplifier position within the array. Three types of amplifiers exist, labeled A, B, or C, which drive either 1, 2, or 4 transmit

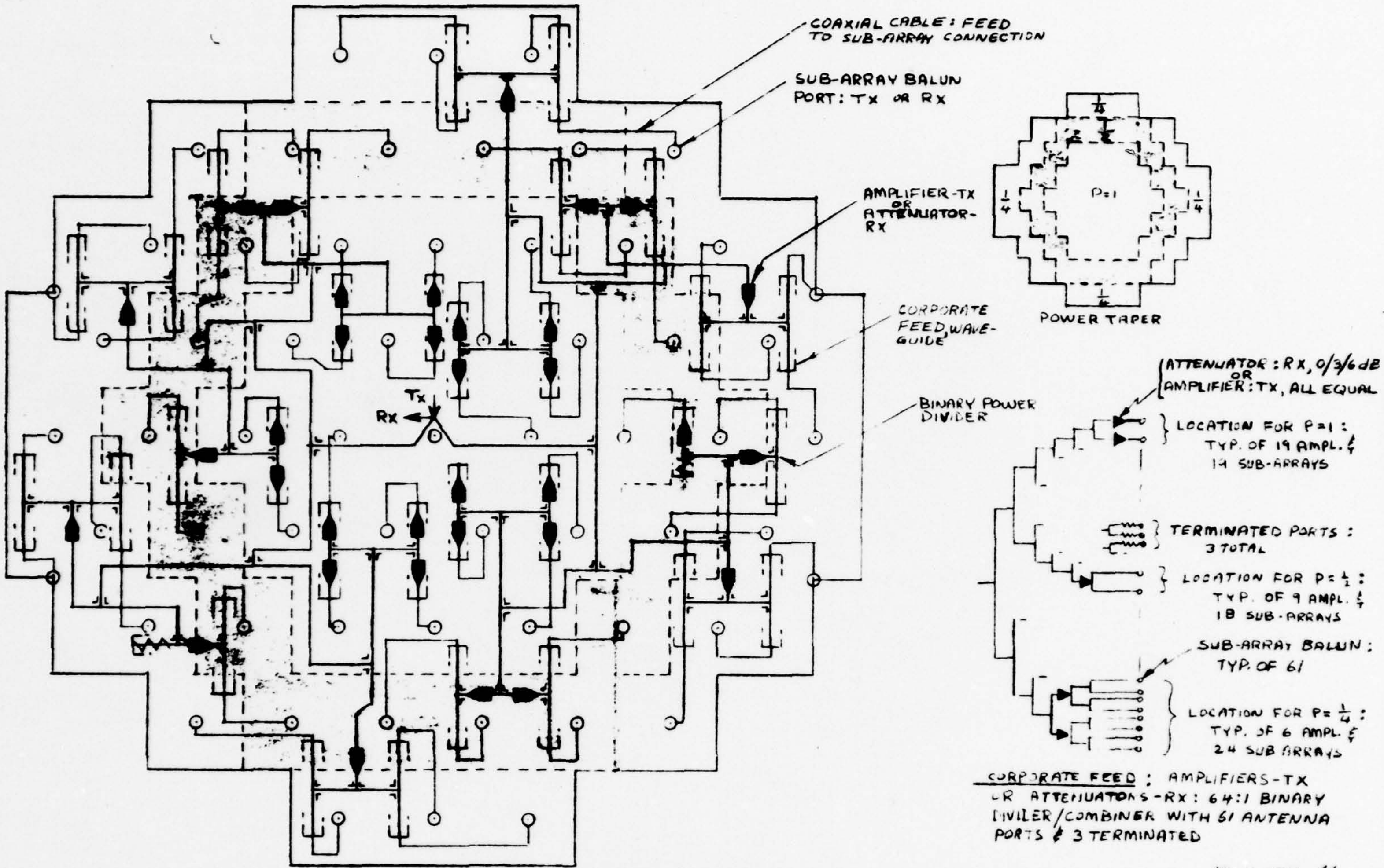


FIGURE 46.

TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION 2 PLACE	3 PLACE	ANGLES	DRAWN BY / CHECKED BY / APPROVED BY	DATE	ITT DEFENSE COMMUNICATIONS DIVISION NUTLEY, NEW JERSEY	SIZE B	CODE IDENT. NO. 28528	ANTENNA LAYOUT - 1KW
							SCALE 1kW	REV. JR. 5/79	SHEET 105

D6216 B REV. 6/73

baluns according to the 3 step taper. The system has 19 'A', 9 'B', and 6 'C' amplifier modules for a total of 34 antenna mounted BPM's. The loss of RF power is given by:

$$P = 10 \log \left(1 - \frac{F}{34} \right) \text{ where } F = \text{\# of failures}$$

and is independent of amplifier position. The loss of antenna gain is a function of the amplifier position since a failure of a 'C' modules removes drive from 4 antenna sub-arrays while an 'A' failure effects only 1 sub-array. The loss in ERP is the sum of both the loss of antenna gain and loss of RF power. Analysis of ERP as a function of amplifier failure has indicated that nine failures distributed around the array (3 'A', 3 'B', and 3 'C' amplifiers) results in 3.13 dB loss in ERP and is thus taken as the criteria for a system failure. For any number of amplifier failures, the largest loss in ERP is always associated with the most 'C' module failures. Take for example the case of six amplifier failures. If all six failures are in the outer region (an unlikely distribution), a loss in ERP of 2.79 dB will result. If all failures are in the center portion of the array, the loss in ERP is only 1.28 dB. The average loss in ERP for all combinations of A, B, and C modules for any number of failures is listed below for up to 10 failures.

Total Number of Failures	Avg. Loss in ERP
1	.30 dB
2	.61 dB
3	.93 dB
4	1.26 dB
5	1.61 dB
6	1.97 dB
7	2.32 dB
8	2.67 dB
9	3.02 dB
10	3.38 dB

Nine failures represents the first case where the average loss in ERP exceeds 3 dB. This topic is discussed in more detail in the Reliability section and includes a detailed tabulation of this analysis.

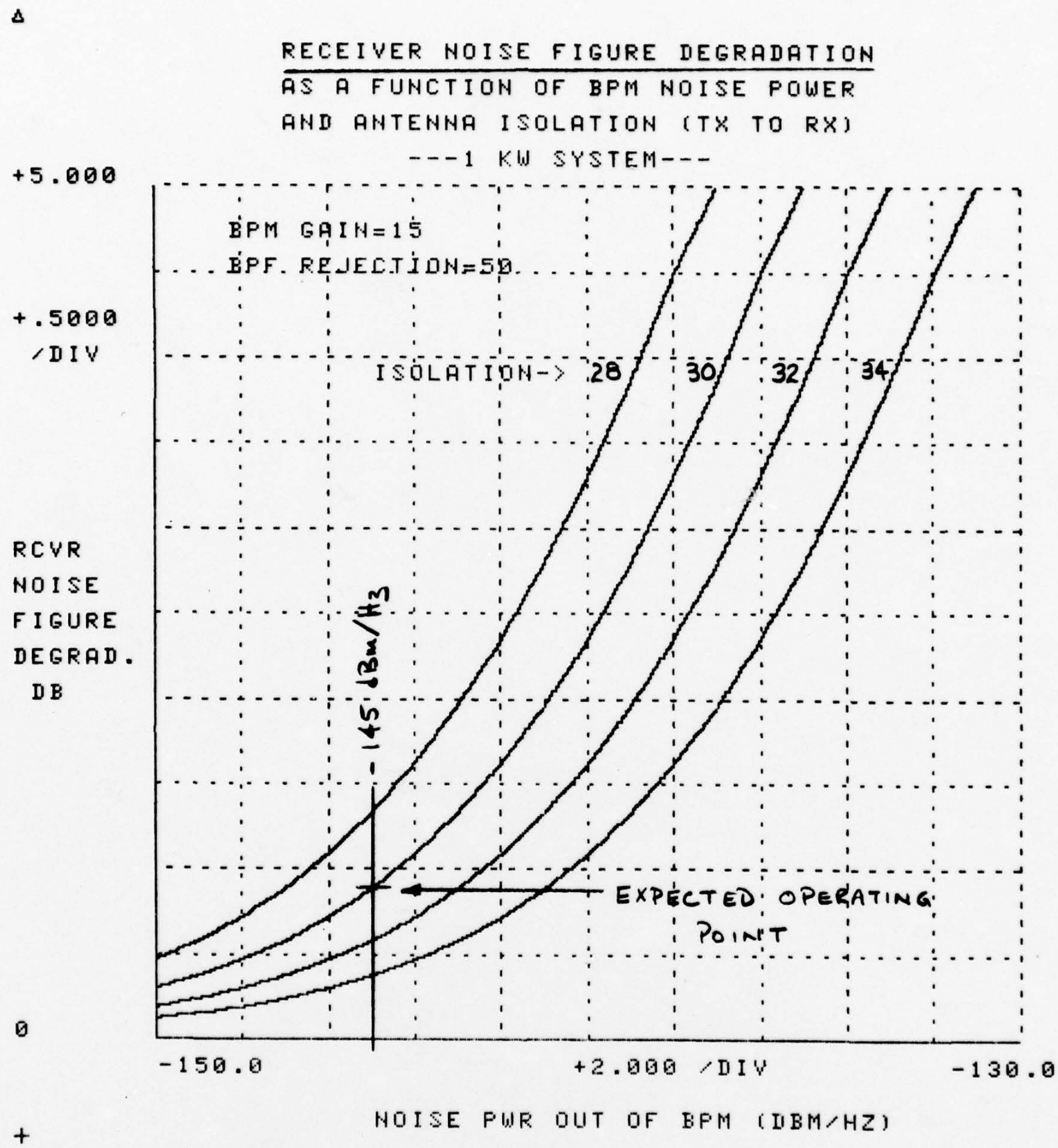
Additionally, with the graceful degradation feature and continuous display of BPM status, a very significant advantage of this system exists when a preventive maintenance schedule is added to the operator's on-site activities.

This maintenance schedule would allow an operator to replace BPM prior to the loss of nine units. This would significantly extend the MTBF of the system by viture of BPM redundancy.

Duplex Operation - To assure that the 1 KW Phased Array Antenna Amplifier does not significantly degrade the duplex operation of the AN/GRC-143 receiver, noise power contributed by the Phased Array transmitter must be limited. The mechanism of this noise contributor is through coupling between the transmit and receive array polarizations.

As in the Scale Model system, there are several sources of noise power contributions which must be investigated: the AN/GRC-143 transmitter, the Driver Amplifier, the IPA, and the antenna mounted BPM's. To reduce the noise contribution of the first three sources, a tunable bandpass filter with 50 dB rejection at $f_o \pm 100$ MHz follows the IPA. The major source of noise would then be the antenna mounted BPM's because their noise is reduced only by the transmit to receive polarization isolation.

A typical noise contribution analysis is shown in Figure 47 for the case of 50 dB filter rejection, 15 dB BPM gain and antenna isolations between 28 and 34 dB. Based upon the Scale Model results, the noise output from a BPM is assumed to be -145 dBm/Hz. At this point, the receiver noise figure degradation is approximately 0.9 dB, the same value budgeted for the Scale Model System. Note that 10 dB more rejection is required from the bandpass filter then in the Scale Model system to account for the additional gain of the 1 KW system. A filter with these characteristics is currently used in the AN/GRC-143 system.



RECEIVER NOISE FIGURE DEGRADATION
AS A FUNCTION OF BPM NOISE POWER
AND ANTENNA ISOLATION (TX TO RX)
---1 KW SYSTEM---
+5.000
+.5000
/DIV
RCVR
NOISE
FIGURE
DEGRAD.
DB
0
BPM GAIN=15
BPF REJECTION=50
ISOLATION-> 28 30 32 34
-145 dBm/Hz
EXPECTED OPERATING POINT
-150.0
+2.000 /DIV
-130.0
NOISE PWR OUT OF BPM (DBM/HZ)

FIGURE 47

System Efficiency - The budgeted system efficiency is 24% (DC - RF) assuming transistor power added efficiency of 35%. Both DC to RF and AC to RF efficiencies were investigated as a function of transistor efficiency as tabulated below. An AC - DC efficiency of 70% was assumed for the power supplies.

Transistor Efficiency	P_{DC} BPM	System Efficiency DC-RF	AC-RF
35%	110 W	24%	16.8%
34%	113.6 W	23.2%	16.3%
30%	129.7 W	20.4%	14.2%

The last case, 14.2% system efficiency, requires 7 KW of AC power which is approximately the same required by present AN/GRC-143 AM-6090 HPA and probably represents the minimum system efficiency to make the system a viable alternative. Since transistors with 30% power added efficiency are presently available, this is not considered to be a risk area.

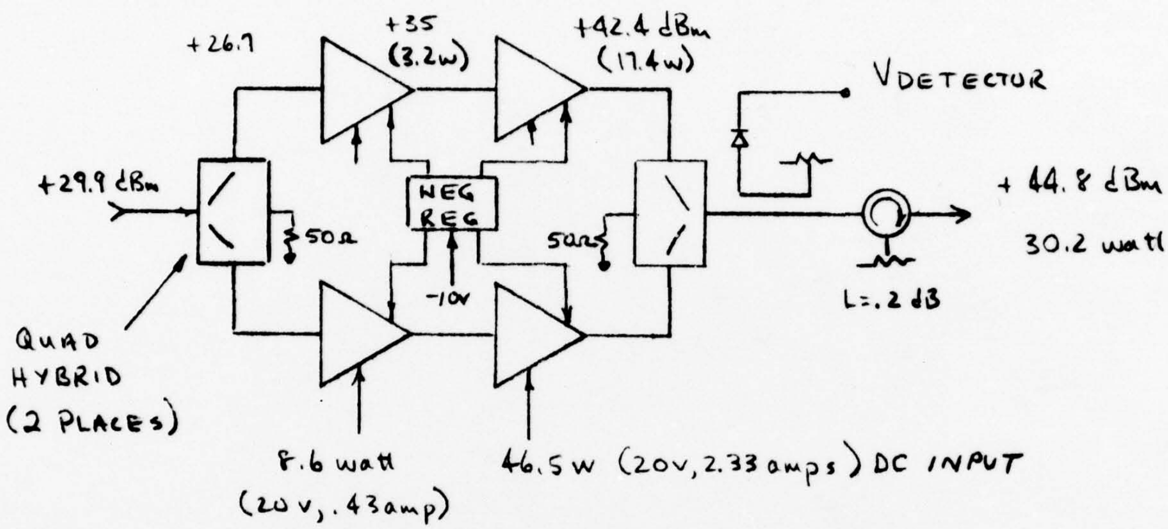
III B. AMPLIFIER DESIGN (BPM) - TRANSISTOR CHARACTERISTICS

The design for the Basic Power Module would be very similar to the concepts developed for the Scale Model amplifier modules. An input quadrature hybrid splits the RF input power to drive a pair of cascaded GaAsFET amplifiers. The output is combined in a second quadrature hybrid before being fed to an low loss output isolator. An output detector similar to the one used for the Scale Model amplifiers is included to monitor output power and provide a signal for the BITE/System Degradation circuitry. A block diagram of the BPM is shown in Figure 48 detailing gain distribution and power consumption. The gain has been kept at approximately 15 dB to minimize the receiver noise figure degradation due to transmitter noise power.

The construction of the BPM would also be similar to that of the Scale Model amplifiers, i.e., microstrip for the RF circuitry and Printed Wiring Board for the negative voltage regulator. The output isolator would be a commercially available low loss stripline unit (loss < 0.2 dB). The amplifiers would be mounted on individual heat sinks machined to provide the walls and bottom of the amplifier chassis. This would reduce the thermal resistance by directly mounting the transistors to the heat sink.

Although alumina was used for the substrate material in the Scale Model amplifiers, the choice for the 1 KW system would depend upon the evaluation of several new, low cost alumina replacements. These materials, versions of which are sold by both Rogers Corp. (Model 6010) and Keene Corp. (Diclad 810) are similar to the Epsilam-10 material evaluated under the initial phases of the Scale Model contract. They offer tighter control on the material de-electric constant and less water absorption and an evaluation similar to that performed on Epsilam-10 would be required. These materials also can be obtained with 1/4 oz. copper plating making fabrication of Lange couplers possible. Of course, the copper would have to be gold plated and this factor would have to be considered in any cost tradeoffs against alumina.

BASIC POWER MODULE FOR 1 KW SYSTEM



PERFORMANCE

POWER OUTPUT	+44.8 dBm (30.2 w)
Gain	14.9 dB
DC POWER	110 watts (20v @ 5.51 amps)
DISSAPATED POWER	80 WATTS
EFFICIENCY	27.4%

35% POWER ADDED EFF ASSUMED FOR TRANSISTORS

TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION 2 PLACE	3 PLACE	ANGLES	1 Kw System - BPM
USED ON		CODE IDENT. NO. 28528	DWG. A SIZE	FIGURE 48
PREPARED BY	DATE			
CHECKED BY	DATE			SHEET 111

In summary, the key design features of the proposed 1 KW Phased Array Antenna Amplifier are as follows:

- 1 KW RF power obtained from 34 equal power (30.2 watts) equal gain (15 dB) BPM's.
- 3 Step Antenna taper obtained by placing BPM's within a low loss waveguide RF distribution network.
- Single Laminate Antenna providing 40 dBi gain and 20 dB sidelobes for both transmit and receive polarizations.
- A 100 watt IPA consisting of 4 BPM's (identical to the antenna mounted BPM's).

Since this design is based upon transistors that are not currently available, a major output of this effort is the required transistor performance to make such a system feasible. These performance specifications are:

	Output Stage Device	Driver Stage Device
Frequency	4.4 - 5.0 GHz	4.4 - 5.0 GHz
Power Output	+42.4 dBm (17.4 watts)	+35 dBm (3.2 watts)
Gain	7.5 dB	8.4 dB
Efficiency (Power Added)	35%	35%
Voltage (operating)	20 volts	20 volts
Failure Rate (Reliability) $^{\Delta}$	5.34×10^{-6} Failures/Hour	
Cost $^{\Delta}$ (1000 pc)	$171	$57

These performance requirements, although not currently available, are not too far from the results being obtained in research laboratories. Power outputs of 15 watts with 30% power added efficiency have recently been reported and work on power GaAsFET's is actively being pursuded in many laboratories. FIJUTSU, NEC, MSC, Raytheon, and TI among others are developing higher power GaAsFET devices.

Δ See Appropriate Section for Backup

1. Antenna Analysis: The critical factors to be analyzed in formulating an antenna design are:

- Effect of geometry on electrical/mechanical performance
- Effect of the number of sub-arrays (independent accesses) on aperture tapering, polarization, packaging, feed systems, loss, and the number of amplifiers.
- Effect of various taper schemes on electrical performance, feed systems, and amplifiers.

Geometry: The basic trade-off is square versus quasi-circular aperture shape. The square geometry has mechanical advantages, due to its X-Y axis symmetries, in packaging and feeding sub-arrays. However, the electrical performance in gain and sidelobes is disadvantageously affected by the large difference between the minimum and maximum distances from array center to edge. That difference makes it particularly difficult to devise a taper scheme which achieves near equal sidelobes in all directions; the significance of large inequalities in sidelobes is a reduction in possible gain for a given aperture side. This was borne out by work done on the scale model which showed through CAD analysis (Page 115) that the quasi-circular aperture attained higher gain and better sidelobe performance than equal area square apertures of either the same or greater aperture steps. In addition, the measured results of the actual antenna (one step taper) showed a difference of 10 dB between the sidelobe levels in the cardinal (minimum edge distance) and intercardinal (maximum edge distance) patterns. The quasi-circular aperture has mechanical disadvantages due to possible complexities in packaging and feed arrangements. However, providing reasonable mechanical arrangements are possible, as is the case, the electrical advantages out weigh the disadvantages. Thus, the quasi-circular is the choice. One remaining consideration - how best to approximate a circle with square sub-arrays is discussed in the taper-CAD section below.

Sub-arrays: The numerous factors, mentioned above, affected by the sub-array size generally involve a trade-off of complexity versus electrical performance, i.e., the smaller the sub-array the more complex the antenna and the better the electrical performance. For example, small sub-arrays allow greater flexibility in choice of

taper steps; or smaller sub-arrays have reduced feed line lengths in the lossy printed media and therefore lower overall losses. However, complexity is a formidable consideration for such a large structure. The final choice was a 4 x 8 dipole sub-array consisting of a balun input, an equal way corporate feed, and 32 dipoles of one polarization. Generally, these are used in pairs to form 8 x 8 sub-arrays uniformly illuminated. The considerations that led to this choice are, in order of importance:

1) 4 x 8 is the largest sub-array which allow dual polarizations on a single laminate, discussed fully below, with binary type corporate feed.
2) Considered in pairs, the aperture can be filled with 61 of 8 x 8 sub-arrays which is sufficiently close to a 64 way external feed system to be compatible; it is highly desireable that a binary type corporate feed be used.
3) A sufficient variety of tapers is possible with 61 sub-arrays.
4) Neither an excessive number of amplifiers, nor excessive powers (projected technology) result from the 61 sub-array choice.
5) Reasonable losses result in the printed corporate feed.

Aperture Taper: To achieve 18 dB sidelobe performance a power taper is required from aperture center to edge. It is to be applied on a sub-array basis such that it must be developed in the external corporate feed, thus each sub-array internally is uniform, and the power varies in steps between sub-arrays. An additional constraint arises from the use of a binary corporate feed in conjunction with all equal power amplifiers, power steps must be from division by 2, i.e., 1, 1/2, 1/4, 1/8, etc. To determine the resulting sidelobe and gain performance a CAD program was used, as for the scale model design. From the scale model results which showed circular apertures to have superior performance, only quasi-circular apertures were evaluated; within this choice two variations were evaluated in the location of the 61 sub-arrays which filled the nominal circle differently. Each of the geometries was evaluated for various tapers and the results are tabulated below with the final choice a 3 step taper - 1:1/2:1/4 in power. Also included is a test case of uniform illumination as a check on the program adaption to the larger array; as expected for a circular aperture the 1st sidelobe levels are 17 to 17.5 dB.

Table of CAD Aperture Taper Evaluation - 1 kw Antenna

Geometry (Ref)	Taper (Power Ratio)	Gain (dB)	Sidelobes (dB)
I (Test Case)	Uniform	43.1	17 - 17.5
I	1:1/4:1/4	41.19	16 - 17
I	1:1/2:1/4	41.68	17 - 17.5
I	1:1/2:1/8	41.12	17 - 18
II	1:1/2:1/8	40.77	17 - 18
III	Uniform	42.94	17 - 17.5
III (Final)	1:1/2:1/4	41.43	20

Ref: I = 61 sub-arrays with row counts: 5 - 6 - 7 - 8 - 9 - 8 - 7 - 6 - 5

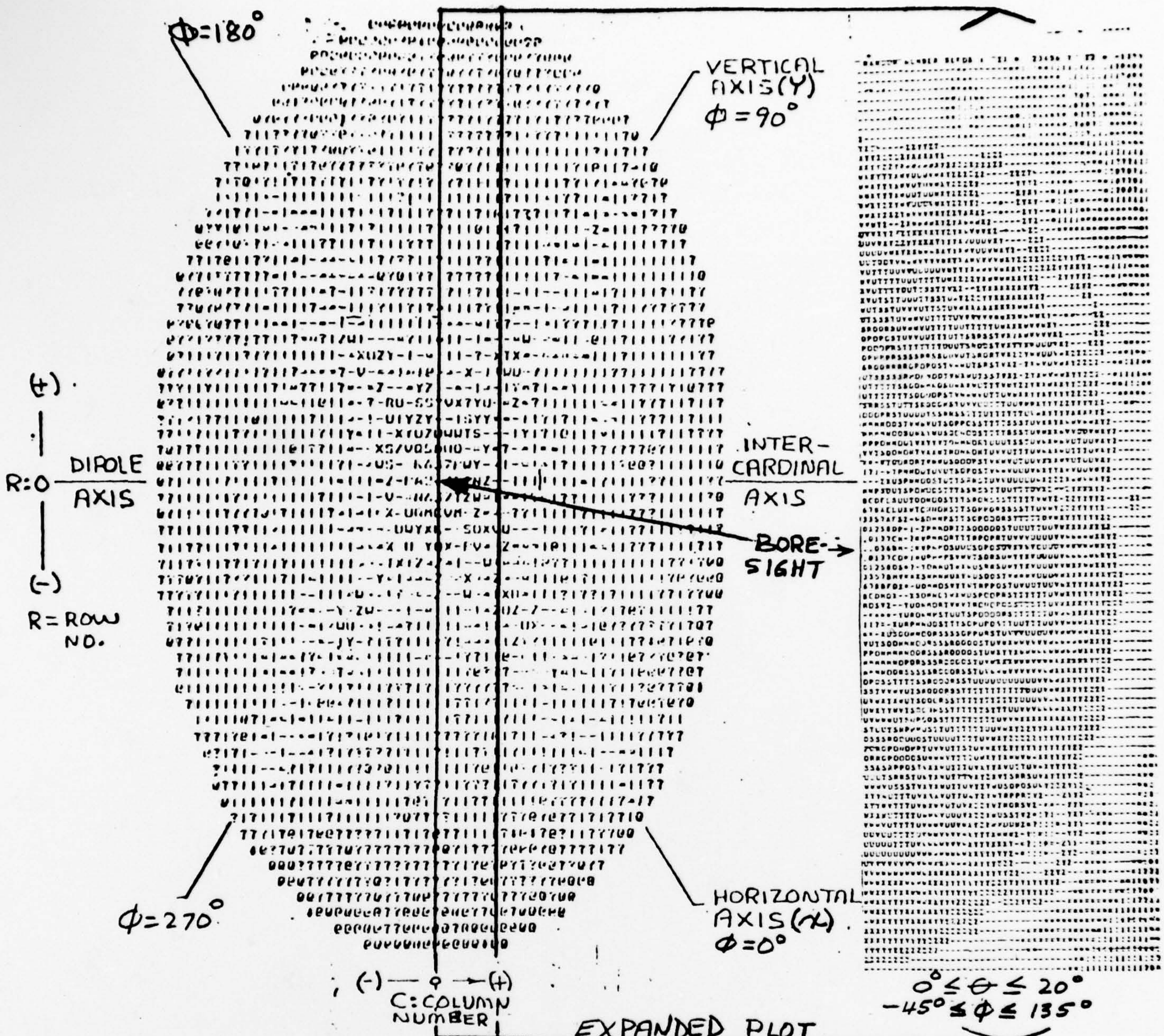
II = 57 sub arrays with row counts: 3 - 6 - 7 - 8 - 9 - 8 - 7 - 6 - 3

III = 61 sub arrays with row counts: 3 - 6 - 8 - 9 - 9 - 9 - 8 - 6 - 3

The indicated choice provides 20 dB sidelobes minimum; this provides margin over the 18 dB requirement. This margin was indicated by the scale model test results which showed 2 dB degradation effects between the calculated and measured sidelobes. Note that lower sidelobe levels than 20 dB can be attained but at the cost of gain.

The final taper choice will be identical for both transmit and receive. Figure 49 & 50 shows a printout of the final computed array pattern.

2. Single Laminate Dual Polarized Techniques: A major change in the method of attaining dual polarization is proposed for the 1 KW antenna. Whereas the scale model used 3 separate aperture size laminates and associated foam spacers arranged in superposition, the 1 KW arrangement requires only a single laminate spaced above a ground plane. The approach was not conceptually evolved for the scale model and was considered a risk approach. The concept is now evolved and the considerable reduction in antenna complexity, cost, and weight mandate its use. For example, the weight of a laminate for the scale model was approximately



PLOTTING FUNCTION

POWER VS SPACE ≹s: θ, Φ

KEY TO DB VALUES OF CHARACTERS ON PLOT

	0 1 2 3 4 5 6 7 8 9
-10	::::::::::::::::::..
0	00112233445566778899
10	AABBCCDDEEFFGGHIJKLMN
20	OPQRSTTUUVVWWXXYYZZ
30	[illegible]
40	||||||||||||||||||||
50	????????????????????
60	[illegible]
70	[illegible]
80	[illegible]
90	[illegible]

$\Phi = 45 + TAN^{-1}\frac{C}{R}$ DEG

$\theta = 1.91^{*}\sqrt{C^2+R^2}$ DEG

R ≡ ROW NO. OF PLOT

C ≡ COLUMN NO. OF PLOT

* PROGRAM CALL-OUT

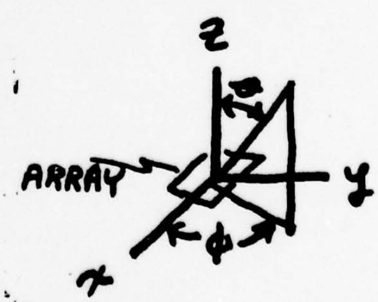


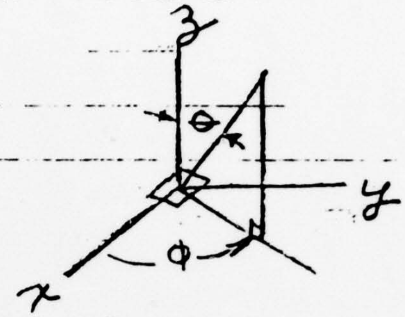
FIG. 49 CAD IKW ANTENNA PATTERN

****** RUN NUMBER 1 ******

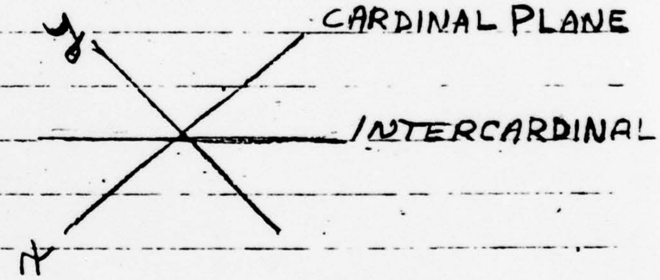
RANDOM NUMBER SEEDS : I1 = 23456 ; I2 = -13579

DB VALUES OF CHARACTERS

	0 1 2 3 4 5 6 7 8 9
-10	:::::::::::::::::::..
0	00112233445566778899
10	AABBCCDDEEFFGHIJKLMN
20	OPQRSSTTUUVVWWXXYYZZ
30	--------============
40	!!!!!!!!!!!!!!!!!!!!
50	????????????????????
60	@@@@@@@@@@@@@@@@@@@@
70	@@@@@@@@@@@@@@@@@@@@



X-Y PROJECTION PLOT



MAGNIFIED-2 QUADRANT:

$0^{\circ} \leq \theta \leq 20$

$0 \leq \phi \leq 180^{\circ}$

FIG. 50 CAD ANTENNA PATTERN PLOT-1KW

10 lbs, or for 3 laminates 30 lbs. Considering that 8 similar sized modules would be required for the 1 KW antenna, a difference of 160 lbs results without the addition of stiffening or support weight. Cost considerations show a similar savings ratio.

The concept uses crossed dipoles on a common center, a well known technique, with a novel arrangement which interlaces 2 corporate feeds, one for each dipole polarization. The interlaced feeds have no crossovers and require no new components or techniques above those used on the scale model. Figure 51 shows a schematic arrangement of the configuration. The generative condition permitting this arrangement is the use and size of the sub-arrays. The use being inherent in at least one polarization to provide multiple access for spatial combining of power, and convenient in the other polarization for implementing the aperture taper on receive. The size (number of dipoles) is limited by the number of feed lines that can be packaged between dipole columns and rows.

In consideration of the electrical performance, the use of a single laminate will provide reduced loss (0.5 to 1.5 dB in scale model) and better VSWR for the receive array, formerly the bottom (buried) array, due to scattering and absorption of the other super imposed laminates. The transmit performance should be at least equal and perhaps slightly improved because of a solid ground plane. The major question in performance is transmit to receive isolation; an improvement is expected for the following reasons:

1. Superior quadrature dipole alignment as controlled by printed circuit techniques rather than mechanical means, including environmental effects. This alignment affects the direct coupling between crossed dipoles due to vectorial resolution. For example, a 1^o mis-alignment results is -35 dB coupling (isolation). $I = -20 \text{ LOG } (\text{SIN} \sphericalangle)$, $\sphericalangle$ angular difference from true quadrature (90^o).
2. Corporate feed lines of the different polarizations are not contiquous and occupy adjacent columns or rows, thus providing no direct coupling mechanisms.
3. Coupling due to scattered waves are considerably reduced by elimination of the two upper laminates, support structures and long balun extensions formerly required to drive the top array.

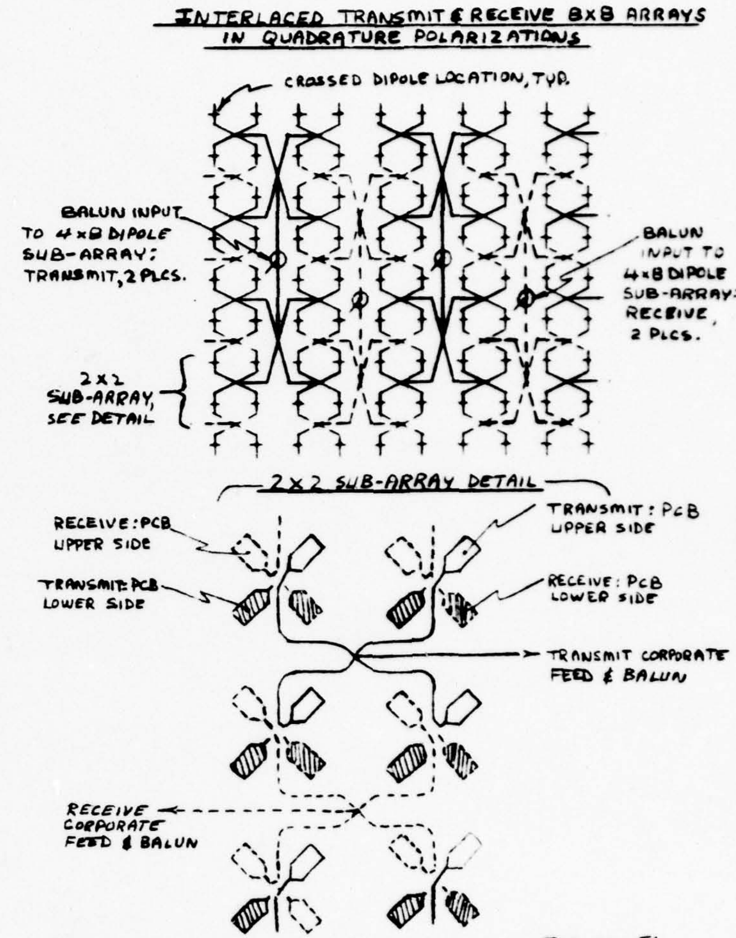


FIGURE 51

TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION 2 PLACE	3 PLACE	ANGLES	DRAWN BY / CHECKED BY / APPROVED BY	DATE	ITT DEFENSE COMMUNICATIONS DIVISION	NUTLEY, NEW JERSEY	SIZE B	CODE IDENT. NO. 28528	DUAL POLARIZATIONS IN SINGLE LAMINATE
								SCALE 1KW	REV. J.R 5/79	SHEET 119

D8215 B REV. 8/73

3. Antenna Concept and Layout: The antenna concept comprises an aperture composed of 61 sub-arrays fed from a 64 way corporate feed: both physically common to each polarization; though electrically isolated. Unused parts of the feed are terminated. Thirty four amplifiers are located at strategic points in the transmit part of the corporate feed to provide a stepped power taper of ratio 1:1/2:1/4 from center to edge aperture sub-arrays. The receive array achieves an identical taper by location of a set of attenuators, matched in impedance and phase, of attenuation ratio 0:3:6 dB. The attenuators can either be located within the corporate feed at locations comparable to the amplifiers, or at the output of each sub-array. Figure 52 shows a pictorial layout of the aperture and corporate feed, and indicates the power distribution across the aperture and the location of amplifiers, or attenuators, within the corporate feed needed to effect that taper.

4. Corporate Feed: The corporate feed system consists of two 64 way dividers: one each for transmit and receive. The basic trade-off in selecting among candidate systems is loss versus weight and complexity for the receive divider. The transmit array is not as critical in loss due to location of amplifiers at the outputs. The alternative media for the feed are: coaxial transmission lines with stripline 2 way dividers, and rectangular waveguide lines and dividers. Each type provides some range in sizes which, again, allows a weight/loss tradeoff. Consider the receive array: if the aperture attains a 2 to 3 dB efficiency (63% to 50%), an additional loss in the corporate feed of 1 dB results in an overall antenna efficiency of 50% to 40%, and a 2 dB feed loss results in 40% to 30% efficiency. Typical reflector antenna achieves 55%, therefore, feed losses of 1 dB or more are unacceptable. Using a rule of thumb in lieu of an exact layout, the total length of all lines in a binary type corporate feed is approximately equal to ten antenna diameters: 100 ft here. A single path length for loss is one diameter: 10 ft. A .250 inch diameter teflon filled coax and associated dividers is compared with aluminum waveguide of either 2 x 1 inch or 2 x 9/16 (half height) cross-section and .064 inch walls below.

Coax Vs. Waveguide 64:1 Corporate Feed

Item	.250 Coax	2 x 1 WG Standard WG	2 x 9/16 WG Half Height
Loss/100 ft (5 GHz)	16.5 dB	2 dB	2.4 dB
Weight/100 ft	10 lbs	45 lbs	38 lbs
Corporate Feed:			
Line Loss: input to any output, 10 ft	1.65 dB	0.2 dB	0.24 dB
Divider Loss: 6 per path	1.5 dB (.25 dB ea)	0.3 dB (.05 dB ea)	0.3 dB (.05 dB ea)
Total Loss	3.15 dB	0.5 dB	0.54 dB
Total Line Wgt: 100 ft	10 lbs	45 lbs	38 lbs
Total Divider Wgt: 63 -2 way units	7.88 lbs (2 oz. ea)	None - Integral to guide	
Total Wgt	17.88 lbs	45 lbs	38 lbs

Although both weights are understated due to non-inclusion of connector and flange weight, the tabulation clearly shows that 2 to 2.5:1 weight advantage of coax is at a 6:1 penalty in loss versus waveguide. More over, beside the loss ratio, the absolute loss of coax is unacceptable for its effect on receive efficiency. Lower loss coax can result in halving the loss with some increase in weight, i.e., 1/2 inch foam heliax: 9 dB/100 ft, 18 lbs/100 ft. Even thus, a total loss of 1.6 dB is still unacceptable for the receive antenna.

The transmit feed could be coaxial because of the compensation of loss in the amplifiers; however, given the commitment to a receive waveguide feed it becomes convenient to use waveguide for transmit. Several alternatives are shown in Figure 53 which "marry" the transmit and receive feeds in a structual unit to reduce weight and refine the packaging and reduce rear antenna complexity. The square tube structure acts as a dual polarized waveguide which simultaneously carries both transmit and receive signals with isolations of 35 to 40 dB typically achieved. The risk area in this approach is the, as yet undemonstrated, availability of a dual mode 2 way power divider. The dual mode feed would weigh 60 lbs, calculated as in the above table; this should be compared to 2 times the tabulated coax weight, or

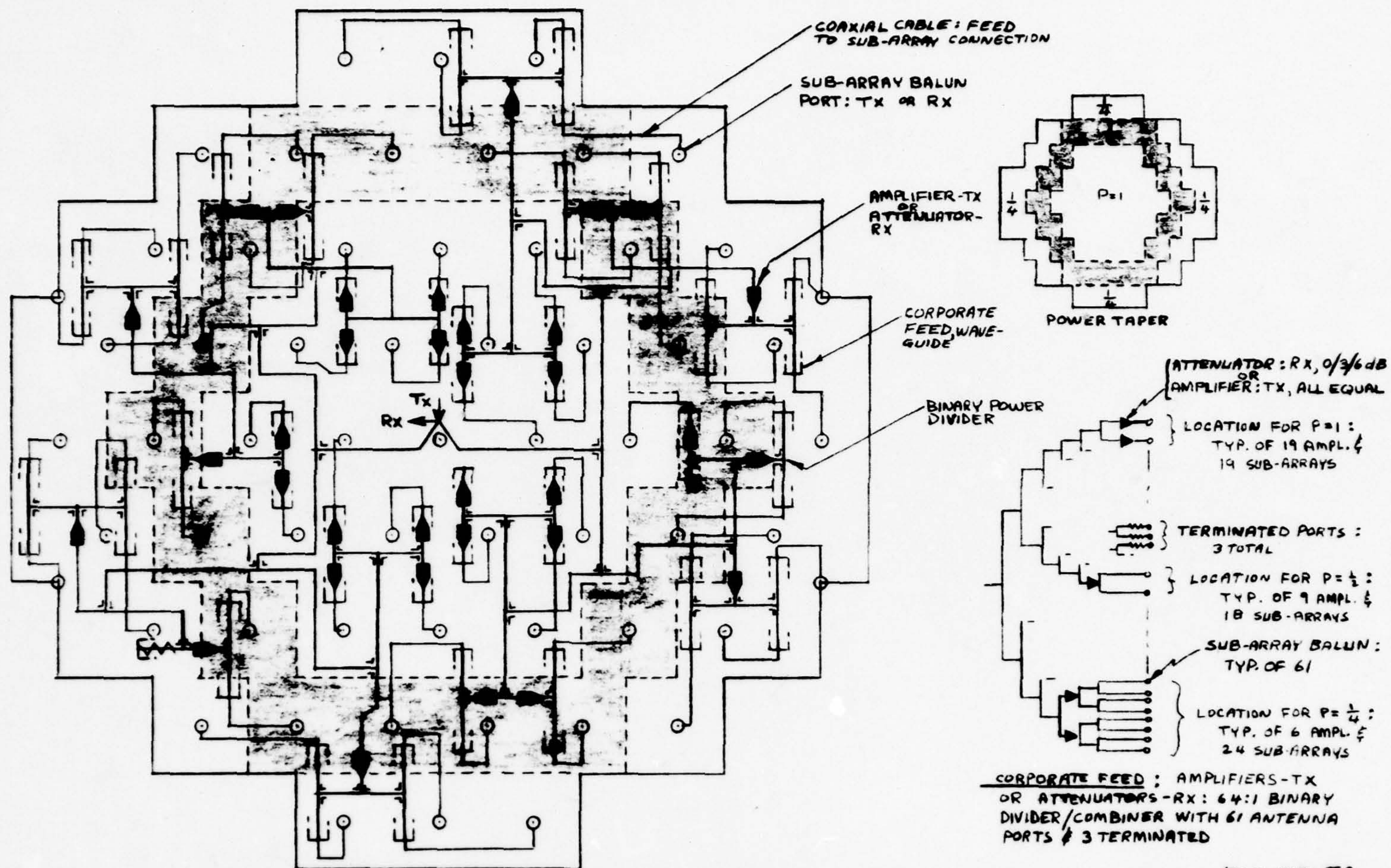
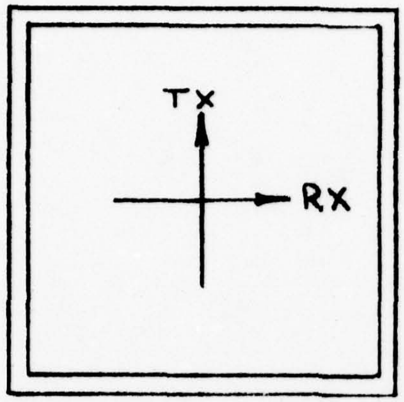


FIGURE 52

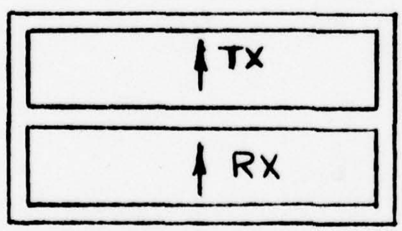
TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION 2 PLACE	3 PLACE	ANGLES	DRAWN BY / DATE CHECKED BY / DATE APPROVED BY / DATE	ITT DEFENSE COMMUNICATIONS DIVISION	NUTLEY, NEW JERSEY	SIZE B	CODE IDENT. NO. 28528	ANTENNA LAYOUT - 1KW
							SCALE 1KW	REV. J.R. 5/79	SHEET 122

D8216 B REV. 5/73



2 X 2 X .064 INCHES
≈ 60 LBS/100 FT, ALUM

DUAL POLARIZED
WAVEGUIDE



2 X 1.064 X .064 INCHES
≈ 63 LBS/100 FT, ALUM

DUAL WAVEGUIDE –
INDEPENDENT POLARIZATIONS

FIGURE 53

ITT DEFENSE COMMUNICATIONS DIVISION	NUTLEY, NEW JERSEY	SIZE B	CODE IDENT. NO. 28528	WAVEGUIDE STRUCTURES
SCALE 1 KW		REV. JR 5/79		SHEET 123

38 lbs, to account for both transmit and receive. The second waveguide scheme uses two half height guides one above the other on the broad wall and with a single thickness common wall. This weighs in at 63 lbs for comparison. The principal advantages of this arrangement are: total isolation between transmit and receive, standard 2-way divider designs.

Input/output requirements either at the 1 and 64 ports or the amplifier locations will use the coax to waveguide probe and back cavity shorting wall, as in standard designs. The physical interface of the feed with the antenna could either be as a one piece, 60 - 70 lb structure, or as a sectionalized assembly patterned to the aperture sections. The single piece approach is attractive only if the waveguide can be used as a stiffening member for the antenna. The sectionalized approach allows the feed weight to be distributed by integration of the feed sections with the aperture sections. This is particularly easy in waveguide since feed lines crossing section boundries can be severed and the opennings flanged without regard to their feed location. Such additional interfaces in waveguide introduce no appreciable electrical degradation.

Waveguide as an entity in itself, and especially as compared to coax, is highly reproducible and at C-Band phase and amplitude errors will be well within the budgeted errors used in the CAD analysis of the scale model antenna: $\pm 20^{o}$ and $\pm$ 0.3 dB. Experience in construction of coaxial cables for the scale model showed errors of up to 14^{o} for cables between .5 to 2 feet. In coax this could be the result of a 7 mil error in length; the comparable waveguide error would require approximately a 14 mil length error which is considered a loose tolerance for waveguide construction. Similarly, the other parameters of loss and VSWR show low ranges of variation in waveguide so that the cumulative errors of the 64 way feed will not exceed the 20^{o}/ .3 dB criteria.

5. <u>Array Sectionalization</u>: Sectionalization of the aperture is the physical configuration of the parts necessary to assemble the required 78 square foot aperture. The size and shape of the sections are determined by the following factors:

- Maximum size is limited by the available substrate (laminate) material: 3 ft x 4 ft.
- Maximum size is limited by weight, handling and storage needs associated with field assembly.
- Shape must be based on integral numbers of sub-array areas in order to preserve the integrity of the printed patterns.
- A minimum number of sections is required to reduce assembly labor and time, consistent with the above restrictions.
- Sections must inter-lock to produce a continuous aperture.
- A minimum number of different shape sections is desireable to reduce the number of artworks required and provide commonality.
- Structural Rigidity, Expansion/Contraction will be greatly influenced by the required environment.

III-D Mechanical Design (Figure 54)

The 1 KW phase array mechanical design would be constructed in a modular fashion, which can be disassembled for transit and storage. It would consist of a four quadrant antenna, a structural antenna support and the sectional 1083 antenna mast used with the AN/TRA-37 10 ft. parabolic dish, standard army tactical tropo antenna.

Antenna Quadrants (Figure 55 & 56)

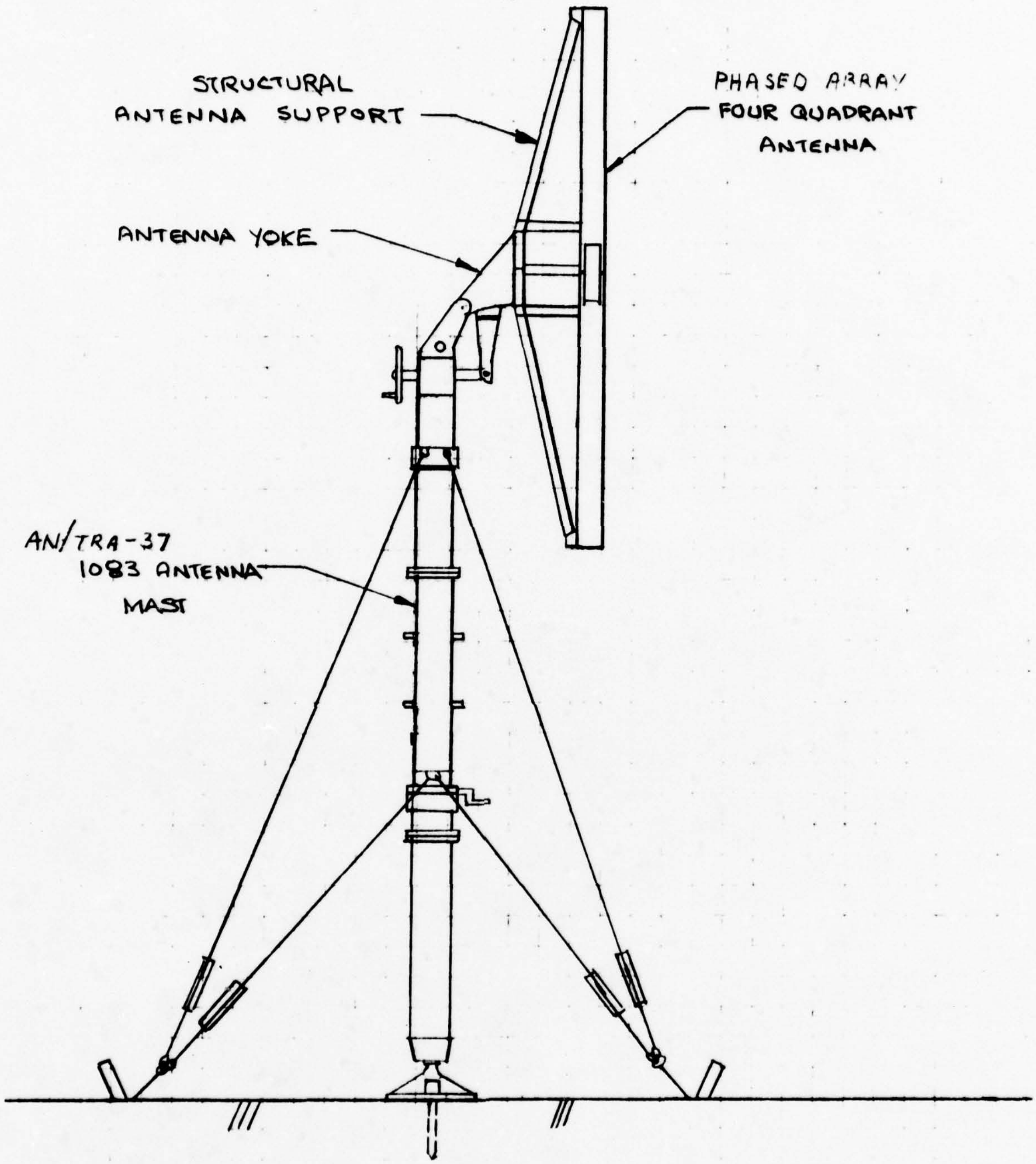
Each antenna quadrant consists of a radome, antenna array, dielectric foam, protective shield, honeycomb support structure (ground plane), amplifiers, waveguide network, and an edge support/sealing containing ring. The four quadrants are held together by a combination of latches located on the periphery of the antenna and structural pins at each interface to assure alignment of the quadrants. Captive quick disconnect waveguide clamps (a single transmit/receive connection at each quadrant) are provided to detach the wave guide network. No loose hardware is required.

The honeycomb will be furnished with inserts so that the amplifiers can be fastened to the surface as in the scale model phased array unit.

All connections between the wave guide network and the antenna will be made using short lengths of semirigid coaxial cable, thus no problem is anticipated with alignment and/or differential expansion between the antenna and the waveguide network due to temperature changes.

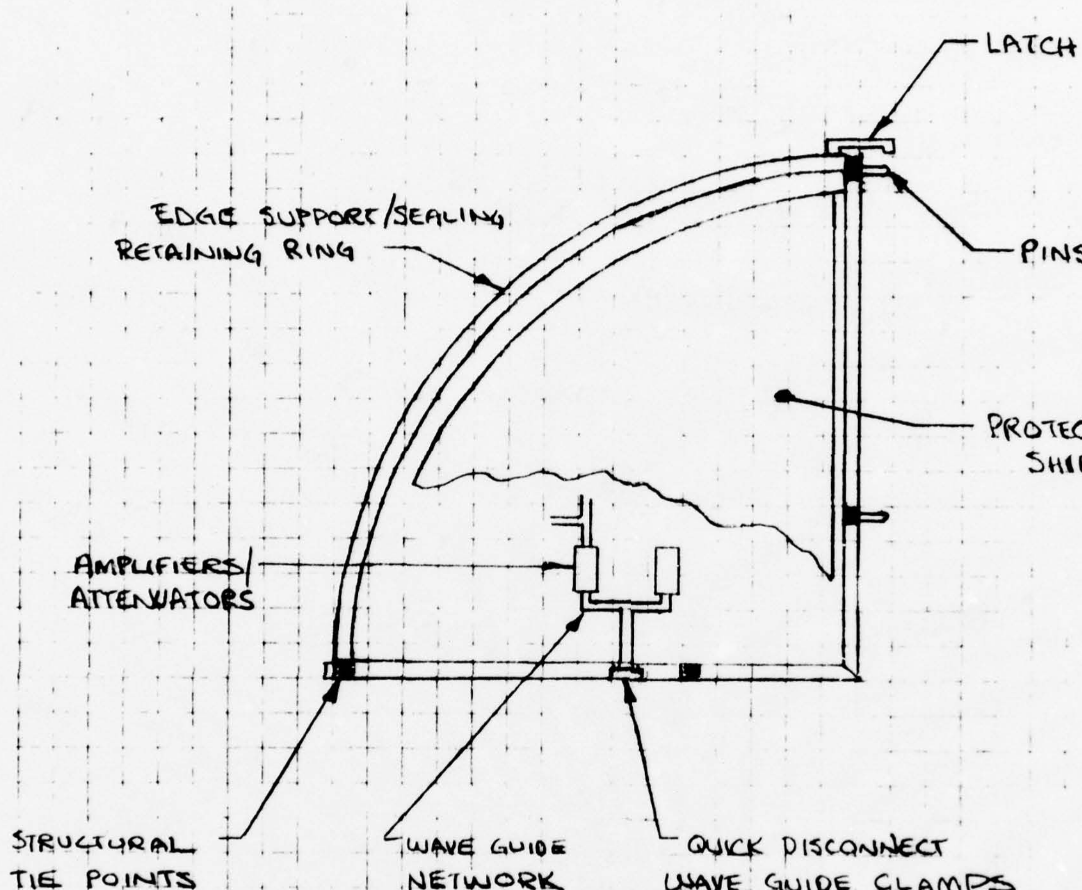
Antenna Support Structure

The antenna support structure will be designed to support the array in the environment and to transfer the loads to the support mast with minimum RF beam deflection. It will be mounted onto the antenna at the eight structural tie points provided on the quadrants. The design will permit the antenna structure to stow within reasonable dimensions due to the use of field separable quadrants.

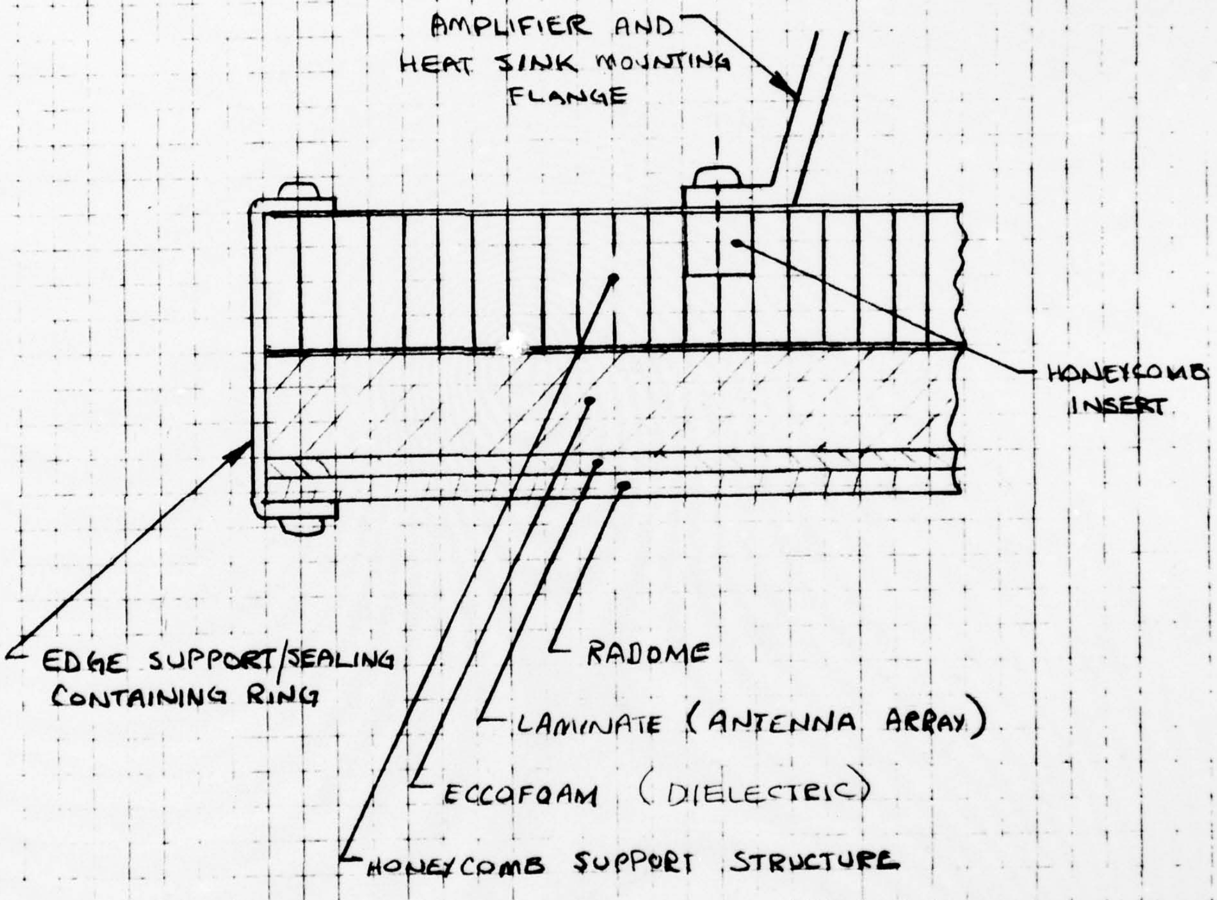


1KW PHASED ARRAY CONCEPT

FIG. 54



TYPICAL ANTENNA QUADRANT
FIG 55



TYPICAL ANTENNA
CROSS SECTION
FIG 56

Antenna Yoke and the 1083 Mast

The antenna yoke will be similar to the one used on AN/TRA-37 but will be made adaptable to the antenna support structure design. The 1083 mast would be used to support the antenna without redesign, since the weight difference can readily be accommodated by the 1083 mast structure.

Thermal Considerations

The 34 amplifiers used on the phase array would dissipate 3400 watts total or 100 watts per amplifier. Cooling would be provided by mounting the amplifier components directly to high efficiency heat sinks. Orientation of the heat sinks would be vertical to maximize the efficiency of heat transfer.

Weight Considerations

The estimated weight of the 1 KW antenna is 525 lbs as shown in Figure 57.

1KW Phase Array Weight Breakdown

Quantity	Item	Weight Each Lbs.	Net Weight Lbs.
	Wave Guide	15	
	Honeycomb	7	
	Antenna Layers	37	
	Amplifiers	25	
	Edge Support	25	
	Protective Shield	12	
	Misc.	4	
4	Total for each antenna quadrant	125	500
1	Structural antenna support	25	25
1	1083 Mast	158	158
		Total Weight	683Lb INCLUDES MAST

FIGURE 57

III E. Reliability Analysis

I. Background

During the initial phase of this program's development, a reliability model was established to predict a militarized (scale model) systems' Mean Time Between Failures (MTBF). This model was based upon 12 Antenna Mounted Basic Power Modules (BPM). As described in Part II System Section, the lack of progress in the Bipolar Transistor area dictated a change (reduction) in scope for the scale model system as delivered. However, the failure rate analysis for the original scale model system provides important information from which to generate a reliability model for the 1 kw system.

Following is a summary of the failure definition for this configuration:

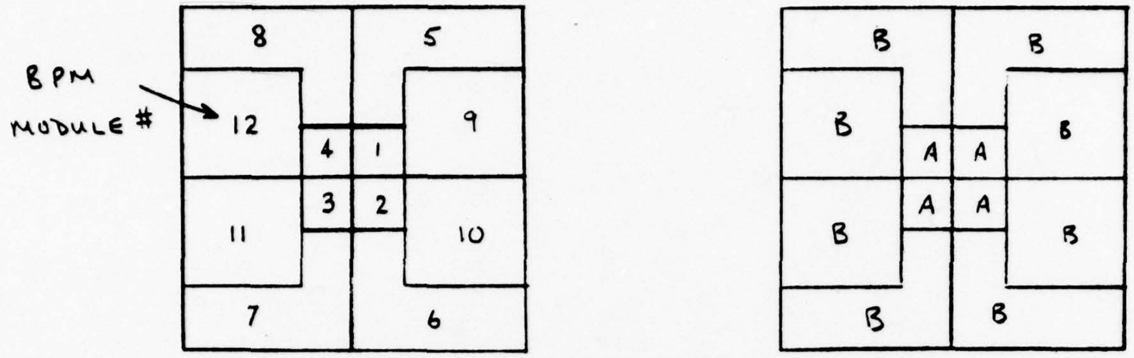
The definition of a system failure is a 3 dB drop in antenna amplifier ERP. Before the system MTBF can be computed, the number of antenna matrix Basic Power Module failures that result in a 3 dB drop in ERP must be determined. To do this, both the loss of power and the loss of antenna gain due to loss of dipoles and beam squinting must be computed. The first component (power) is straightforward and is given by:

$$P = 10 \log \left[1 - \frac{\text{No. of failures}}{12} \right]$$

To compute the loss of antenna gain, a computer program was written to calculate the dipole element pattern by direct integration of the sinusoidal current along the dipole length. A vectorial summation of all array elements is performed at any far field point providing a non-approximate analysis for any shape array, and grid or error pattern. The bore sight gain is computed including loss of gain due to beam squinting.

The loss of antenna gain due to BPM failures was analyzed and the results are shown in Figure 58 for up to 4 total failures. The gains listed are the computed directivity at 4.7 GHz. Included is a drawing of the antenna array with the distribution of the 12 BPM's. The total loss in ERP is also shown and is a maximum of 3.06 dB for any three BPM failures.

TRANSMIT ANTENNA (SCALE MODEL)



FAILURES	A	B	DIRECTIVITY @ 4.7 GHz	ΔG	ΔP	ΔERP (-dB)
	0	0	34.04 dB	—	—	—
1 FAILURE	1	0	33.96	.08 dB	.38 dB	.46 dB
	0	1	33.51	.53 dB	↓	.91 dB
2 FAILURES	2	0	33.89	.15 dB	.79 dB	.94 dB
	1	1	33.41	.63 dB		1.42 dB
	0	2	32.91	1.13 dB	↓	1.92 dB
3 FAILURES	3	0	33.83	.21 dB	1.25 dB	1.46 dB
	2	1	33.33	.71 dB		1.96 dB
	1	2	32.79	1.25 dB		2.50 dB
	0	3	32.23	1.81 dB	↓	3.06 dB
4 FAILURES	4	0	33.79	.25 dB	1.76 dB	2.01 dB
	3	1	33.26	.78 dB		2.54 dB
	2	2	32.68	1.36 dB		3.12 dB
	1	3	32.08	1.96 dB		3.72 dB
	0	4	31.42	2.62 dB	↓	4.38 dB

TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION 2 PLACE	DECIMAL DIMENSION 3 PLACE	ANGLES	PHASED ARRAY - ΔERP

USED ON

PREPARED BY DATE

CHECKED BY DATE

CODE IDENT. NO. 28528

DWG. A SIZE

FIGURE 58

SHEET 133

It was found that the loss of antenna gain due to beam squinting was a negligible component of the total loss of gain. As a result, the loss in gain due to the failure of BPM's 5, 9 and 10 for example, is equal to the loss of gain due to the failure of BPM's 6, 9 and 12. Refer to Figure 58. for BPM module numbers. Because of this, the antenna array can be broken down into 4 inner (A) and 8 outer (B) BPM's. The loss in ERP has been listed versus the number of failures of these A and B modules.

For this configuration four BPM failures were taken as the failure criteria resulting in a system failure (-3 dB ERP).

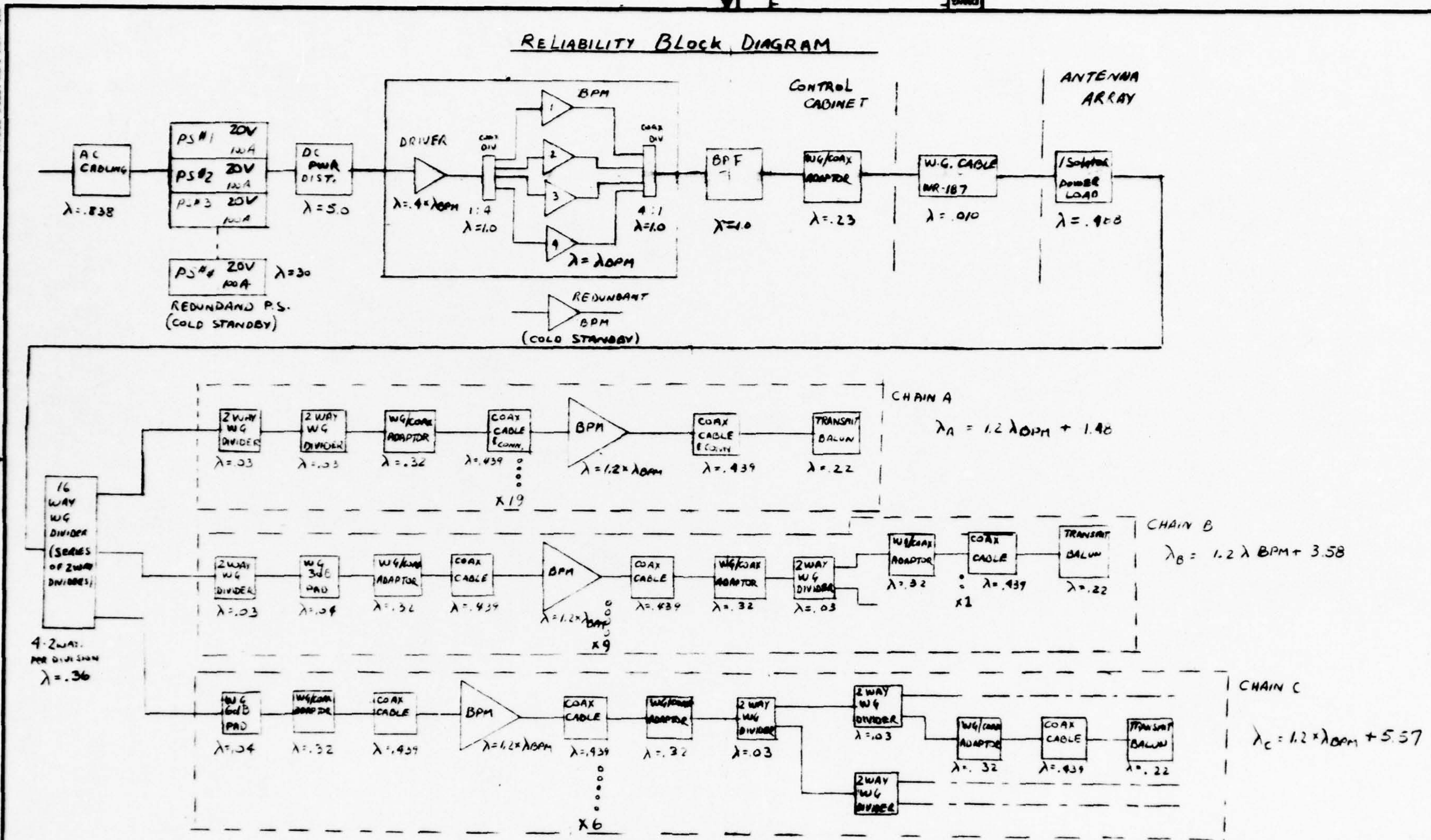
II 1 KW System

The purpose of a Reliability Analysis for the proposed 1 kw system is to establish failure rates for the major system components. The target is to provide a failure rate distribution which results in a system MTBF of 4000 hours minimum.

To accomplish this, a reliability block diagram of the 1 kw system is shown in Figure 59. This diagram contains all the major RF components, DC power supplies and distribution networks. In the area of the antenna BPM, the 3 step antenna taper requires 3 different RF distribution chains (all BPM are identical). For the application of RF power to the Transmit Array, redundancy is provided by having, as cold standby, one additional IPA BPM and one additional DC power supply. Thus, when either a power supply or IPA BPM fail, the spare units can be switched in with minimal impact on traffic. The graceful degradation feature of this system resides in the fact that several antenna BPM can fail prior to a loss of 3 dB in ERP (Failure Criteria).

Thus, the initial task is to determine the quantity and position of failures, their effects on loss of transmitter power and antenna gain. As per the previous analysis, the loss in power is calculated as:

$$P_{RF} = 10 \log \left(1 - \frac{\text{No. of Failures}}{34}\right)$$



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APPROVED BY | DATE

ITT DEFENSE COMMUNICATIONS DIVISION, NUTLEY, NEW JERSEY

SIZE B | CODE IDENT. NO. 28528 | FIGURE 59

SCALE | REV. | SHEET 135

Where 34 is the total number of antenna BPM's. Relative position of the BPM within the array has no bearing on the loss of power.

The loss of antenna gain is dependent upon position since the taper design provides for different areas of illumination depending upon position of the BPM within this distribution network.

The loss of gain (ΔG) versus position is determined via the computer program previously described but expanded for this configuration.

Figure 60 summarizes the degradation in ERP vs. BPM failure. This chart assumes that a BPM failure results in a total loss of RF energy from that BPM. This is a pessimistic approach since it does not take into account a partial failure in a BPM. This partial failure would result if only one input stage, one output stage, or one chain (input driving an output) failed. The other side would still provide power, 6 dB lower than normal (due to the final stage power combiner).

Calculation of the MTBF for this system follows these guide lines:

- Desired system MTBF is 4000 hours.
- 20% (1/5) of this 4000 hours ($\lambda = \frac{1}{4000} = 250 \times 10^{-6}$ failure/hours) are allocated to system components not shown (FR = 50×10^{-6} failures/hours).
- Redundancy is provided for the DC power supplies and IPA Basic Power Modules.
- IPA BPM has a lower failure rate than the antenna BPM due to forced air cooling in the control cabinet.
- IPA Driver has a lower failure rate than an IPA BPM due to its lower DC power requirements, lower transistor channel termperature, and forced air cooling.
- Failure rates, λ_I for passive components are taken from MIL-STD-Handbook 217B at 40^{o}C ambient temperature.
- Failure rate for power supplies based upon Militarized switching units of comparable capacity.

----ERP ANALYSIS---
1 KW SYSTEM

TOTAL NUMBER OF FAILURES=0

FAILURES A	B	C	ΔP (dB)	ΔG (dB)	ΔERP (dB)
.0	.0	.0	-.00	-.00	-.00

AVG LOSS IN ERP(dB)=-.01

TOTAL NUMBER OF FAILURES=1

FAILURES A	B	C	ΔP (dB)	ΔG (dB)	ΔERP (dB)
.0	.0	1.0	-.13	-.28	-.41
.0	1.0	.0	-.13	-.16	-.29
1.0	.0	.0	-.13	-.07	-.20

AVG LOSS IN ERP(dB)=-.3

TOTAL NUMBER OF FAILURES=2

FAILURES A	B	C	ΔP (dB)	ΔG (dB)	ΔERP (dB)
.0	.0	2.0	-.26	-.57	-.83
.0	1.0	1.0	-.26	-.44	-.71
.0	2.0	.0	-.26	-.32	-.58
1.0	.0	1.0	-.26	-.35	-.62
1.0	1.0	.0	-.26	-.23	-.49
2.0	.0	.0	-.26	-.14	-.41

AVG LOSS IN ERP(dB)=-.61

TOTAL NUMBER OF FAILURES=3

FAILURES A	B	C	ΔP (dB)	ΔG (dB)	ΔERP (dB)
.0	.0	3.0	-.40	-.88	-1.28
.0	1.0	2.0	-.40	-.75	-1.15
.0	2.0	1.0	-.40	-.62	-1.02
.0	3.0	.0	-.40	-.49	-.89
1.0	.0	2.0	-.40	-.65	-1.06
1.0	1.0	1.0	-.40	-.52	-.92
1.0	2.0	.0	-.40	-.40	-.80
2.0	.0	1.0	-.40	-.43	-.83
2.0	1.0	.0	-.40	-.31	-.71
3.0	.0	.0	-.40	-.22	-.62

AVG LOSS IN ERP(dB)=-.93

TOTAL NUMBER OF FAILURES=4

FAILURES A	B	C	ΔP (dB)	ΔG (dB)	ΔERP (dB)
.0	.0	4.0	-.54	-1.21	-1.76
.0	1.0	3.0	-.54	-1.07	-1.61
.0	2.0	2.0	-.54	-.93	-1.48
.0	3.0	1.0	-.54	-.79	-1.34
.0	4.0	.0	-.54	-.66	-1.20
1.0	.0	3.0	-.54	-.97	-1.52
1.0	1.0	2.0	-.54	-.83	-1.38
1.0	2.0	1.0	-.54	-.70	-1.24
1.0	3.0	.0	-.54	-.57	-1.11
2.0	.0	2.0	-.54	-.74	-1.28
2.0	1.0	1.0	-.54	-.60	-1.15
2.0	2.0	.0	-.54	-.47	-1.02
3.0	.0	1.0	-.54	-.51	-1.06

FIGURE 60

3.0	1.0	.0	-.54	-.38	-.92
4.0	.0	.0	-.54	-.29	-.83

AVG LOSS IN ERP(dB)=-1.26

TOTAL NUMBER OF FAILURES=5

FAILURES			ΔP	ΔG	ΔERP
A	B	C	(dB)	(dB)	(dB)
.0	.0	5.0	-.69	-1.57	-2.26
.0	1.0	4.0	-.69	-1.42	-2.11
.0	2.0	3.0	-.69	-1.27	-1.96
.0	3.0	2.0	-.69	-1.12	-1.81
.0	4.0	1.0	-.69	-.98	-1.67
.0	5.0	.0	-.69	-.84	-1.53
1.0	.0	4.0	-.69	-1.31	-2.00
1.0	1.0	3.0	-.69	-1.17	-1.86
1.0	2.0	2.0	-.69	-1.02	-1.71
1.0	3.0	1.0	-.69	-.88	-1.57
1.0	4.0	.0	-.69	-.74	-1.43
2.0	.0	3.0	-.69	-1.06	-1.76
2.0	1.0	2.0	-.69	-.92	-1.61
2.0	2.0	1.0	-.69	-.78	-1.48
2.0	3.0	.0	-.69	-.65	-1.34
3.0	.0	2.0	-.69	-.82	-1.52
3.0	1.0	1.0	-.69	-.69	-1.38
3.0	2.0	.0	-.69	-.55	-1.24
4.0	.0	1.0	-.69	-.59	-1.28
4.0	1.0	.0	-.69	-.46	-1.15
5.0	.0	.0	-.69	-.36	-1.06

AVG LOSS IN ERP(dB)=-1.61

TOTAL NUMBER OF FAILURES=6

FAILURES			ΔP	ΔG	ΔERP
A	B	C	(dB)	(dB)	(dB)
.0	.0	6.0	-.84	-1.94	-2.79
.0	1.0	5.0	-.84	-1.78	-2.63
.0	2.0	4.0	-.84	-1.63	-2.47
.0	3.0	3.0	-.84	-1.48	-2.32
.0	4.0	2.0	-.84	-1.32	-2.17
.0	5.0	1.0	-.84	-1.18	-2.02
.0	6.0	.0	-.84	-1.03	-1.87
1.0	.0	5.0	-.84	-1.67	-2.52
1.0	1.0	4.0	-.84	-1.52	-2.36
1.0	2.0	3.0	-.84	-1.37	-2.21
1.0	3.0	2.0	-.84	-1.22	-2.06
1.0	4.0	1.0	-.84	-1.07	-1.92
1.0	5.0	.0	-.84	-.93	-1.77
2.0	.0	4.0	-.84	-1.41	-2.26
2.0	1.0	3.0	-.84	-1.26	-2.11
2.0	2.0	2.0	-.84	-1.12	-1.96
2.0	3.0	1.0	-.84	-.97	-1.81
2.0	4.0	.0	-.84	-.83	-1.67
3.0	.0	3.0	-.84	-1.16	-2.00
3.0	1.0	2.0	-.84	-1.01	-1.86
3.0	2.0	1.0	-.84	-.87	-1.71
3.0	3.0	.0	-.84	-.73	-1.57
4.0	.0	2.0	-.84	-.91	-1.76
4.0	1.0	1.0	-.84	-.77	-1.61
4.0	2.0	.0	-.84	-.63	-1.48
5.0	.0	1.0	-.84	-.67	-1.52
5.0	1.0	.0	-.84	-.54	-1.38

FIGURE 60

6.0	.0	.0	-.84	-.44	-1.28

AVG LOSS IN ERP(dB)=-1.97

TOTAL NUMBER OF FAILURES=7

FAILURES A	B	C	ΔP (dB)	ΔG (dB)	ΔERP (dB)
.0	1.0	6.0	-1.00	-2.18	-3.18
.0	2.0	5.0	-1.00	-2.02	-3.02
.0	3.0	4.0	-1.00	-1.85	-2.85
.0	4.0	3.0	-1.00	-1.69	-2.69
.0	5.0	2.0	-1.00	-1.54	-2.54
.0	6.0	1.0	-1.00	-1.38	-2.38
.0	7.0	.0	-1.00	-1.23	-2.23
1.0	.0	6.0	-1.00	-2.06	-3.07
1.0	1.0	5.0	-1.00	-1.90	-2.90
1.0	2.0	4.0	-1.00	-1.74	-2.74
1.0	3.0	3.0	-1.00	-1.58	-2.58
1.0	4.0	2.0	-1.00	-1.43	-2.43
1.0	5.0	1.0	-1.00	-1.27	-2.27
1.0	6.0	.0	-1.00	-1.12	-2.12
2.0	.0	5.0	-1.00	-1.79	-2.79
2.0	1.0	4.0	-1.00	-1.63	-2.63
2.0	2.0	3.0	-1.00	-1.47	-2.47
2.0	3.0	2.0	-1.00	-1.32	-2.32
2.0	4.0	1.0	-1.00	-1.17	-2.17
2.0	5.0	.0	-1.00	-1.02	-2.02
3.0	.0	4.0	-1.00	-1.52	-2.52
3.0	1.0	3.0	-1.00	-1.36	-2.36
3.0	2.0	2.0	-1.00	-1.21	-2.21
3.0	3.0	1.0	-1.00	-1.06	-2.06
3.0	4.0	.0	-1.00	-.92	-1.92
4.0	.0	3.0	-1.00	-1.25	-2.26
4.0	1.0	2.0	-1.00	-1.11	-2.11
4.0	2.0	1.0	-1.00	-.96	-1.96
4.0	3.0	.0	-1.00	-.81	-1.81
5.0	.0	2.0	-1.00	-1.00	-2.00
5.0	1.0	1.0	-1.00	-.86	-1.86
5.0	2.0	.0	-1.00	-.71	-1.71
6.0	.0	1.0	-1.00	-.75	-1.76
6.0	1.0	.0	-1.00	-.61	-1.61
7.0	.0	.0	-1.00	-.51	-1.52

AVG LOSS IN ERP(dB)=-2.32

TOTAL NUMBER OF FAILURES=8

FAILURES A	B	C	ΔP (dB)	ΔG (dB)	ΔERP (dB)
.0	2.0	6.0	-1.17	-2.43	-3.60
.0	3.0	5.0	-1.17	-2.26	-3.42
.0	4.0	4.0	-1.17	-2.09	-3.25
.0	5.0	3.0	-1.17	-1.92	-3.09
.0	6.0	2.0	-1.17	-1.76	-2.92
.0	7.0	1.0	-1.17	-1.59	-2.76
.0	8.0	.0	-1.17	-1.44	-2.60
1.0	1.0	6.0	-1.17	-2.31	-3.47
1.0	2.0	5.0	-1.17	-2.14	-3.30
1.0	3.0	4.0	-1.17	-1.97	-3.13
1.0	4.0	3.0	-1.17	-1.80	-2.97
1.0	5.0	2.0	-1.17	-1.64	-2.81
1.0	6.0	1.0	-1.17	-1.48	-2.65
1.0	7.0	.0	-1.17	-1.33	-2.49

FIGURE 60

2.0	.0	6.0	-1.17	-2.19	-3.35
2.0	1.0	5.0	-1.17	-2.02	-3.18
2.0	2.0	4.0	-1.17	-1.85	-3.02
2.0	3.0	3.0	-1.17	-1.69	-2.85
2.0	4.0	2.0	-1.17	-1.53	-2.69
2.0	5.0	1.0	-1.17	-1.37	-2.54
2.0	6.0	.0	-1.17	-1.22	-2.38
3.0	.0	5.0	-1.17	-1.90	-3.07
3.0	1.0	4.0	-1.17	-1.74	-2.90
3.0	2.0	3.0	-1.17	-1.57	-2.74
3.0	3.0	2.0	-1.17	-1.42	-2.58
3.0	4.0	1.0	-1.17	-1.26	-2.43
3.0	5.0	.0	-1.17	-1.11	-2.27
4.0	.0	4.0	-1.17	-1.62	-2.79
4.0	1.0	3.0	-1.17	-1.46	-2.63
4.0	2.0	2.0	-1.17	-1.31	-2.47
4.0	3.0	1.0	-1.17	-1.15	-2.32
4.0	4.0	.0	-1.17	-1.00	-2.17
5.0	.0	3.0	-1.17	-1.35	-2.52
5.0	1.0	2.0	-1.17	-1.20	-2.36
5.0	2.0	1.0	-1.17	-1.05	-2.21
5.0	3.0	.0	-1.17	-.90	-2.06
6.0	.0	2.0	-1.17	-1.09	-2.26
6.0	1.0	1.0	-1.17	-.94	-2.11
6.0	2.0	.0	-1.17	-.79	-1.96
7.0	.0	1.0	-1.17	-.84	-2.00
7.0	1.0	.0	-1.17	-.69	-1.86
8.0	.0	.0	-1.17	-.59	-1.76

AVG LOSS IN ERP(dB)=-2.67

TOTAL NUMBER OF <u>FAILURES=9</u>

FAILURES			ΔP	ΔG	ΔERP
A	B	C	(dB)	(dB)	(dB)
.0	3.0	6.0	-1.34	-2.70	-4.03
.0	4.0	5.0	-1.34	-2.52	-3.85
.0	5.0	4.0	-1.34	-2.34	-3.67
.0	6.0	3.0	-1.34	-2.16	-3.50
.0	7.0	2.0	-1.34	-1.99	-3.32
.0	8.0	1.0	-1.34	-1.82	-3.15
.0	9.0	.0	-1.34	-1.65	-2.99
1.0	2.0	6.0	-1.34	-2.57	-3.90
1.0	3.0	5.0	-1.34	-2.39	-3.72
1.0	4.0	4.0	-1.34	-2.21	-3.55
1.0	5.0	3.0	-1.34	-2.04	-3.37
1.0	6.0	2.0	-1.34	-1.87	-3.20
1.0	7.0	1.0	-1.34	-1.70	-3.04
1.0	8.0	.0	-1.34	-1.54	-2.87
2.0	1.0	6.0	-1.34	-2.44	-3.78
2.0	2.0	5.0	-1.34	-2.26	-3.60
2.0	3.0	4.0	-1.34	-2.09	-3.42
2.0	4.0	3.0	-1.34	-1.92	-3.25
2.0	5.0	2.0	-1.34	-1.75	-3.09
2.0	6.0	1.0	-1.34	-1.59	-2.92
2.0	7.0	.0	-1.34	-1.42	-2.76
3.0	.0	6.0	-1.34	-2.31	-3.65
3.0	1.0	5.0	-1.34	-2.14	-3.47
3.0	2.0	4.0	-1.34	-1.97	-3.30
3.0	3.0	3.0	-1.34	-1.80	-3.13
3.0	4.0	2.0	-1.34	-1.63	-2.97
3.0	5.0	1.0	-1.34	-1.47	-2.81

FIGURE 60

3.0	6.0	.0	-1.34	-1.31	-2.65
4.0	.0	5.0	-1.34	-2.02	-3.35
4.0	1.0	4.0	-1.34	-1.85	-3.18
4.0	2.0	3.0	-1.34	-1.68	-3.02
4.0	3.0	2.0	-1.34	-1.52	-2.85
4.0	4.0	1.0	-1.34	-1.36	-2.69
4.0	5.0	.0	-1.34	-1.20	-2.54
5.0	.0	4.0	-1.34	-1.73	-3.07
5.0	1.0	3.0	-1.34	-1.57	-2.90
5.0	2.0	2.0	-1.34	-1.40	-2.74
5.0	3.0	1.0	-1.34	-1.25	-2.58
5.0	4.0	.0	-1.34	-1.09	-2.43
6.0	.0	3.0	-1.34	-1.45	-2.79
6.0	1.0	2.0	-1.34	-1.29	-2.63
6.0	2.0	1.0	-1.34	-1.14	-2.47
6.0	3.0	.0	-1.34	-.98	-2.32
7.0	.0	2.0	-1.34	-1.18	-2.52
7.0	1.0	1.0	-1.34	-1.03	-2.36
7.0	2.0	.0	-1.34	-.88	-2.21
8.0	.0	1.0	-1.34	-.92	-2.26
8.0	1.0	.0	-1.34	-.77	-2.11
9.0	.0	.0	-1.34	-.67	-2.00

AVG LOSS IN ERP(dB)=-3.03

TOTAL NUMBER OF FAILURES=10

FAILURES A	B	C	ΔP (dB)	ΔG (dB)	ΔERP (dB)
.0	4.0	6.0	-1.51	-2.98	-4.49
.0	5.0	5.0	-1.51	-2.79	-4.30
.0	6.0	4.0	-1.51	-2.60	-4.11
.0	7.0	3.0	-1.51	-2.41	-3.93
.0	8.0	2.0	-1.51	-2.23	-3.74
.0	9.0	1.0	-1.51	-2.05	-3.57
1.0	3.0	6.0	-1.51	-2.84	-4.36
1.0	4.0	5.0	-1.51	-2.65	-4.17
1.0	5.0	4.0	-1.51	-2.47	-3.98
1.0	6.0	3.0	-1.51	-2.28	-3.80
1.0	7.0	2.0	-1.51	-2.11	-3.62
1.0	8.0	1.0	-1.51	-1.93	-3.44
1.0	9.0	.0	-1.51	-1.76	-3.27
2.0	2.0	6.0	-1.51	-2.71	-4.22
2.0	3.0	5.0	-1.51	-2.52	-4.03
2.0	4.0	4.0	-1.51	-2.34	-3.85
2.0	5.0	3.0	-1.51	-2.16	-3.67
2.0	6.0	2.0	-1.51	-1.98	-3.50
2.0	7.0	1.0	-1.51	-1.81	-3.32
2.0	8.0	.0	-1.51	-1.64	-3.15
3.0	1.0	6.0	-1.51	-2.58	-4.09
3.0	2.0	5.0	-1.51	-2.39	-3.90
3.0	3.0	4.0	-1.51	-2.21	-3.72
3.0	4.0	3.0	-1.51	-2.03	-3.55
3.0	5.0	2.0	-1.51	-1.86	-3.37
3.0	6.0	1.0	-1.51	-1.69	-3.20
3.0	7.0	.0	-1.51	-1.52	-3.04
4.0	.0	6.0	-1.51	-2.44	-3.96
4.0	1.0	5.0	-1.51	-2.26	-3.78
4.0	2.0	4.0	-1.51	-2.09	-3.60
4.0	3.0	3.0	-1.51	-1.91	-3.42
4.0	4.0	2.0	-1.51	-1.74	-3.25
4.0	5.0	1.0	-1.51	-1.57	-3.09

FIGURE 60

4.0	6.0	.0	-1.51	-1.41	-2.92
5.0	.0	5.0	-1.51	-2.14	-3.65
5.0	1.0	4.0	-1.51	-1.96	-3.47
5.0	2.0	3.0	-1.51	-1.79	-3.30
5.0	3.0	2.0	-1.51	-1.62	-3.13
5.0	4.0	1.0	-1.51	-1.46	-2.97
5.0	5.0	.0	-1.51	-1.29	-2.81
6.0	.0	4.0	-1.51	-1.84	-3.35
6.0	1.0	3.0	-1.51	-1.67	-3.18
6.0	2.0	2.0	-1.51	-1.50	-3.02
6.0	3.0	1.0	-1.51	-1.34	-2.85
6.0	4.0	.0	-1.51	-1.18	-2.69
7.0	.0	3.0	-1.51	-1.55	-3.07
7.0	1.0	2.0	-1.51	-1.39	-2.90
7.0	2.0	1.0	-1.51	-1.23	-2.74
7.0	3.0	.0	-1.51	-1.07	-2.58
8.0	.0	2.0	-1.51	-1.27	-2.79
8.0	1.0	1.0	-1.51	-1.12	-2.63
8.0	2.0	.0	-1.51	-.96	-2.47
9.0	.0	1.0	-1.51	-1.00	-2.52
9.0	1.0	.0	-1.51	-.85	-2.36
10.0	.0	.0	-1.51	-.74	-2.26

AVG LOSS IN ERP(dB)=-3.39

TOTAL NUMBER OF FAILURES=11

FAILURES			ΔP	ΔG	ΔERP
A	B	C	(dB)	(dB)	(dB)
.0	5.0	6.0	-1.70	-3.28	-4.98
.0	6.0	5.0	-1.70	-3.08	-4.77
.0	7.0	4.0	-1.70	-2.88	-4.57
.0	8.0	3.0	-1.70	-2.68	-4.38
.0	9.0	2.0	-1.70	-2.49	-4.19
1.0	4.0	6.0	-1.70	-3.13	-4.83
1.0	5.0	5.0	-1.70	-2.93	-4.63
1.0	6.0	4.0	-1.70	-2.74	-4.44
1.0	7.0	3.0	-1.70	-2.55	-4.24
1.0	8.0	2.0	-1.70	-2.36	-4.06
1.0	9.0	1.0	-1.70	-2.17	-3.87
2.0	3.0	6.0	-1.70	-2.99	-4.69
2.0	4.0	5.0	-1.70	-2.80	-4.49
2.0	5.0	4.0	-1.70	-2.60	-4.30
2.0	6.0	3.0	-1.70	-2.41	-4.11
2.0	7.0	2.0	-1.70	-2.23	-3.93
2.0	8.0	1.0	-1.70	-2.05	-3.74
2.0	9.0	.0	-1.70	-1.87	-3.57
3.0	2.0	6.0	-1.70	-2.85	-4.55
3.0	3.0	5.0	-1.70	-2.66	-4.36
3.0	4.0	4.0	-1.70	-2.47	-4.17
3.0	5.0	3.0	-1.70	-2.28	-3.98
3.0	6.0	2.0	-1.70	-2.10	-3.80
3.0	7.0	1.0	-1.70	-1.92	-3.62
3.0	8.0	.0	-1.70	-1.75	-3.44
4.0	1.0	6.0	-1.70	-2.71	-4.41
4.0	2.0	5.0	-1.70	-2.52	-4.22
4.0	3.0	4.0	-1.70	-2.34	-4.03
4.0	4.0	3.0	-1.70	-2.15	-3.85
4.0	5.0	2.0	-1.70	-1.97	-3.67
4.0	6.0	1.0	-1.70	-1.80	-3.50
4.0	7.0	.0	-1.70	-1.63	-3.32
5.0	.0	6.0	-1.70	-2.58	-4.28

FIGURE 60

INCOMPLETE LISTING OF 11 FAILURES

Calculation

In reviewing the mathematics for determining the Mean Time Between Failure (MTBF) of the Basic Power Module (BPM), a simplified reliability block diagram was prepared (from Figure 59, Figure 61). As MTBF is the inverse of the sum of the failure rates in a serial model, the first task was to convert each of the 5 block groups into an equivalent failure rate.

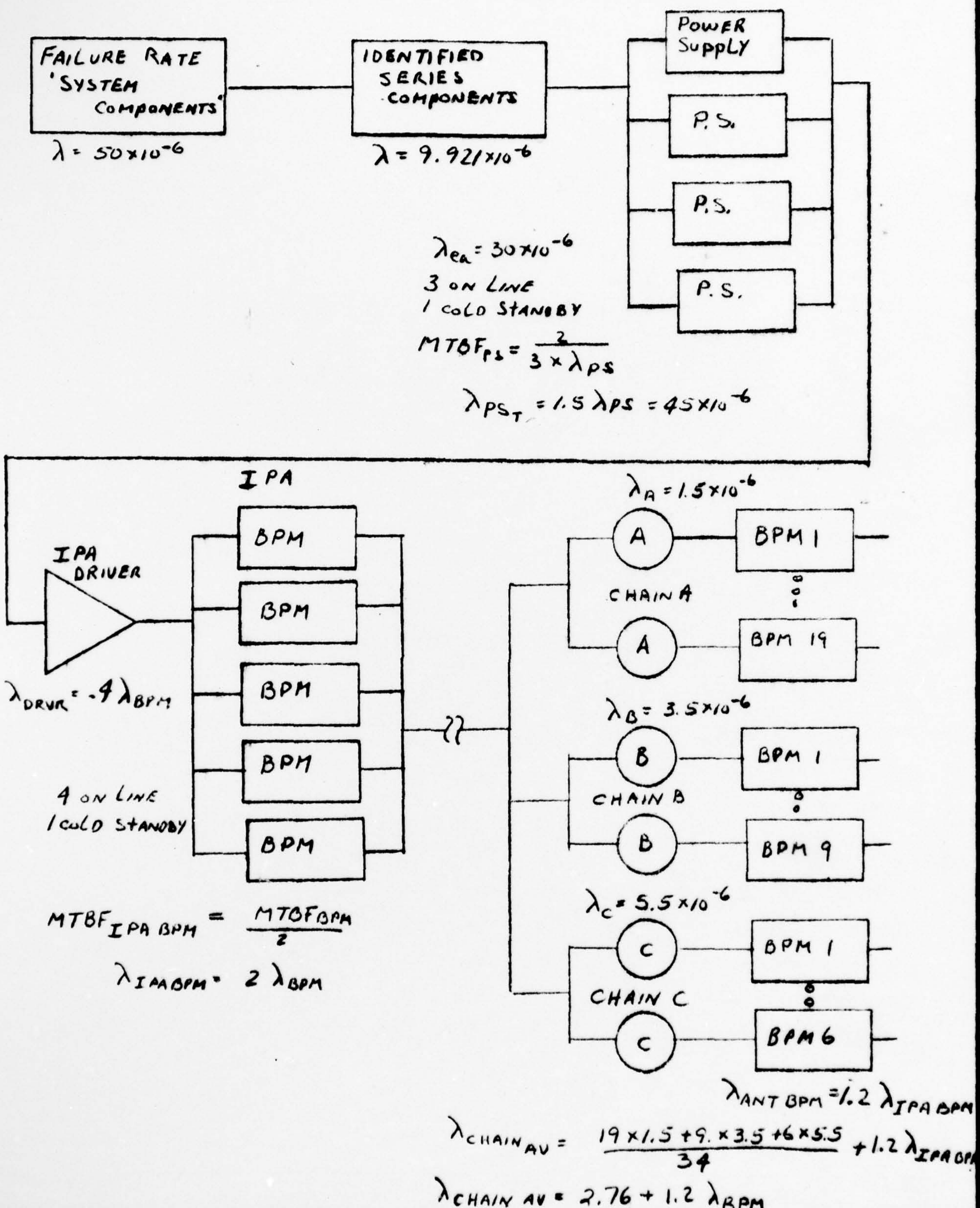
Power Supply - From any standard reliability handbook, the MTBF for a 3 out of 4 configuration with cold standby redundancy is 2/3 x unit MTBF. Therefore, the equivalent failure rate for the power supply group is a failure rate equal to 1.5 x the failure rate of a power supply.

IPA - For the IPA amplifier group with a 4 out of 5 configuration with cold standby redundancy, the equivalent failure rate is 2 x the failure rate of a Basic Power Module (BPM).

Antenna Amplifier Chain - The equivalent failure rate for the 34 amplifier chains group was determined from the definition of success and the allowable number of failures for no greater than a 3 dB loss in ERP.

Within the antenna array there are 34 amplifiers. These are grouped into 3 types, each with a slightly different failure rate in series with a basic power module and providing a slightly different amount of signal loss when it fails. From the computer run of loss per quantity of each of the 3 types of amplifier chains (A, B, & C), Figure 60 the type and number of "success" states was evaluated (Figure 62). Success states arise from the combinations of up to 12 failures. All combinations of 0, 1, 2, 3, 4, 5, and 6 failures provide a loss less than 3 dB therefore 100% success states. Of all combinations of 7 failures, 99.996% provide a "success" condition. Of all combinations of 8 failures, 99.227% provide a "success" condition. Of all combinations of 9, 10, 11, and 12 failures, the "success" percentage of state probabilities are 86.944%, 45.000%, 7.855%, and 0.133%, respectively.

SIMPLIFIED RELIABILITY BLOCK DIAGRAM



ITT DEFENSE COMMUNICATIONS DIVISION — NUTLEY, NEW JERSEY

DRAWING NUMBER

PREPARED BY	SIZE	CODE IDENT NO.	DWG. NO.
CHECKED BY	A	28528	FIGURE 61
		REV.	SHEET 144

CALCULATION OF SUCCESS STATES

# of BPM Failures	Total # of States	Total # of Failed States	% of Success States
0	1	0	100%
1	34	0	100%
2	c 561	0	100%
3	5,984	0	100%
4	46,376	0	100%
5	278,256	0	100%
6	1,344,904	0	100%
7	5,379,616	216	99.996%
8	18,156,204	140,346	99.227%
9	52,451,256	6,847,998	86.944%

$$\text{Total \# of States} = \frac{34!}{R!(34-R)!}$$

R = Total # of Failed States (BPM)

$$\text{Total \# of Failed States} = \frac{19!}{R_A!(19-R_A)!} \times \frac{9!}{R_B!(9-R_B)!} \times \frac{6!}{R_C!(6-R_C)!}$$

Summation over the # of combinations giving a 3 dB loss in ERP.

$$\text{\% of Success States} = \frac{\text{Total \# of States} - \text{Total \# of Failed States}}{\text{Total \# of States}}$$

FIGURE 62

From a human factors point of view to minimize interpretation by a user, all conditions of up to and including 8 failures can be considered a success state. In evaluating the MTBF of the amplifier array, an assumption had to be made to simplify the mathematics. This assumption is that there is an average series failure rate in each chain. This number was determined by dividing the total series failure rate of all 34 chains by 34.

The equation for the MTBF of the amplifier array mathematically considering a success of all states up to and including 8 failures is:

$$MTBF_{AA} = \sum_{r=0}^{8} \frac{MTBF}{r} \text{ Chain} = \frac{MTBF\ (BPM_{AA} + SERIES\quad)}{3.3085}$$

Using the assumption that the failure rate of the BPM in the antenna array is 1.2 x the failure rate of the physically identical BPM in the IPA, the failure rate equation is:

$$FR_{AA} = \lambda_{AA} = 3.3085 \times (\lambda \text{ BPM} \times 1.2 + 2.76^*)$$

$*2.76 = \lambda$ AV of components other than BPM

Further, considering that the failure rate of the driver amplifier is 0.4 x the failure rate of a IPA BPM, the failure rate of identified series items is 9.921×10^{-6}. The reserve failure rate is 50×10^{-6}, and the failure rate of a power supply is 30×10^{-6}. For a 4000 hours MTBF, the series failure rate is 250×10^{-6} failures/hour. Therefore, the equation to determine the BPM failure rate is:

$$250 \times 10^{-6} = 50 \times 10^{-6} + 9.921 \times 10^{-6} + 1.5 \times 30 \times 10^{-6} + (0.4 \times \lambda \text{BPM}) + 2 \times \lambda \text{ BPM} + 3.3085 \times (1.2 \times \lambda \text{BPM}) + 2.76 \times 10^{-6}$$

$$\lambda \text{BPM} = 136.07899/6.3702 = 21.362 \times 10^{-6} \text{ failures/hour}$$

$$MTBF_{BPM} = 46{,}812 \text{ hours}$$

For 4 devices per BPM, assuming each is equally likely to fail: λ device = λ BPM/4 = 5.34×10^{-6} failures/hours. A failure rate (λ) of 5.34×10^{-6}/hour is comparable to a JAN TXV devices with an LTPD equal to 5.

A recent document from RADC "Reliability Prediction Models for Microwave Solid State Devices", RADC-TR-79-50, April 1979 reports on GaAsFET Devices reliability testing. The report cites the tests performed by various manufacturers (page 47):

"A report on a solid state amplifier study for power amplifiers (GaAsFET) (Reference 16) indicates a range of from 1.6×10^7 hours to 3.6×10^7 hours MTBF for 3 types of power GaAsFETs at 150°C junction temperature. A test conducted on twenty devices, operated at a junction temperature of 125°C for 1000 hours was completed with no catastrophic failures (See Reference 17). One report, evaluating three types of devices, predicts an MTBF of 10^8 hours at junction temperatures of 100°C (See Reference 18).

A study of low noise microwave GaAsFETs shows the predicted MTBF for the devices to be 2×10^8 hours at 100°C (See Reference 19). From an evaluation of these reports it becomes evident that various manufacturers, using different designs and processes for manufacturing the devices, produce reliability data which varies very much and lacks uniformity. The failure rate to be developed then requires an evaluation of the data available and engineering judgment in the determination of the reliability of the device. Junction temperatures obtained are a result of thermal conductivity of the device, the amount of current adjusted in the device and the ambient temperature of the air around the device. Nominal operating junction temperature is in the order of 150°C. If it is considered that devices operated at 150°C junction temperature have a predicted MTBF of between 0.03×10^6 hours and 5×10^7 hours dependent on the type of device, then a value of 5×10^6 hours can be postulate for a GaAsFET that was operated at a 25°C ambient temperature and a 50 percent stress. This results in a failure rate of 0.2 failures/10^6 hours at that one point (See Reference 20)."

Thus, a required failure rate of 5.34×10^{-6} failures / hour (or 5.34 failures in 10^6 hours) has already been demonstrated for power GaAsFETs operated at high junction (channel) temperatures.

As further testing of devices occurs prediction models will be better defined, enabling determination of failure rates based on application, power level, and quality factors. These could then be used to confidently determine device failure rates for a given application based on a larger sample, very similar to the manner in which silicon bipolar transistors are characterized.

In summary, the reliability model assumed for the 1 KW system requires the use of a GaAsFET device with a failure rate currently attainable.

III F. BITE SYSTEM - Refer to Figure 63

The function of the BITE system is to monitor and display the status and operation of the Phased Array Antenna Amplifier. It performs this task by sensing the output of each BPM and continuously updating a LED (Light Emitting Diode) display with this information.

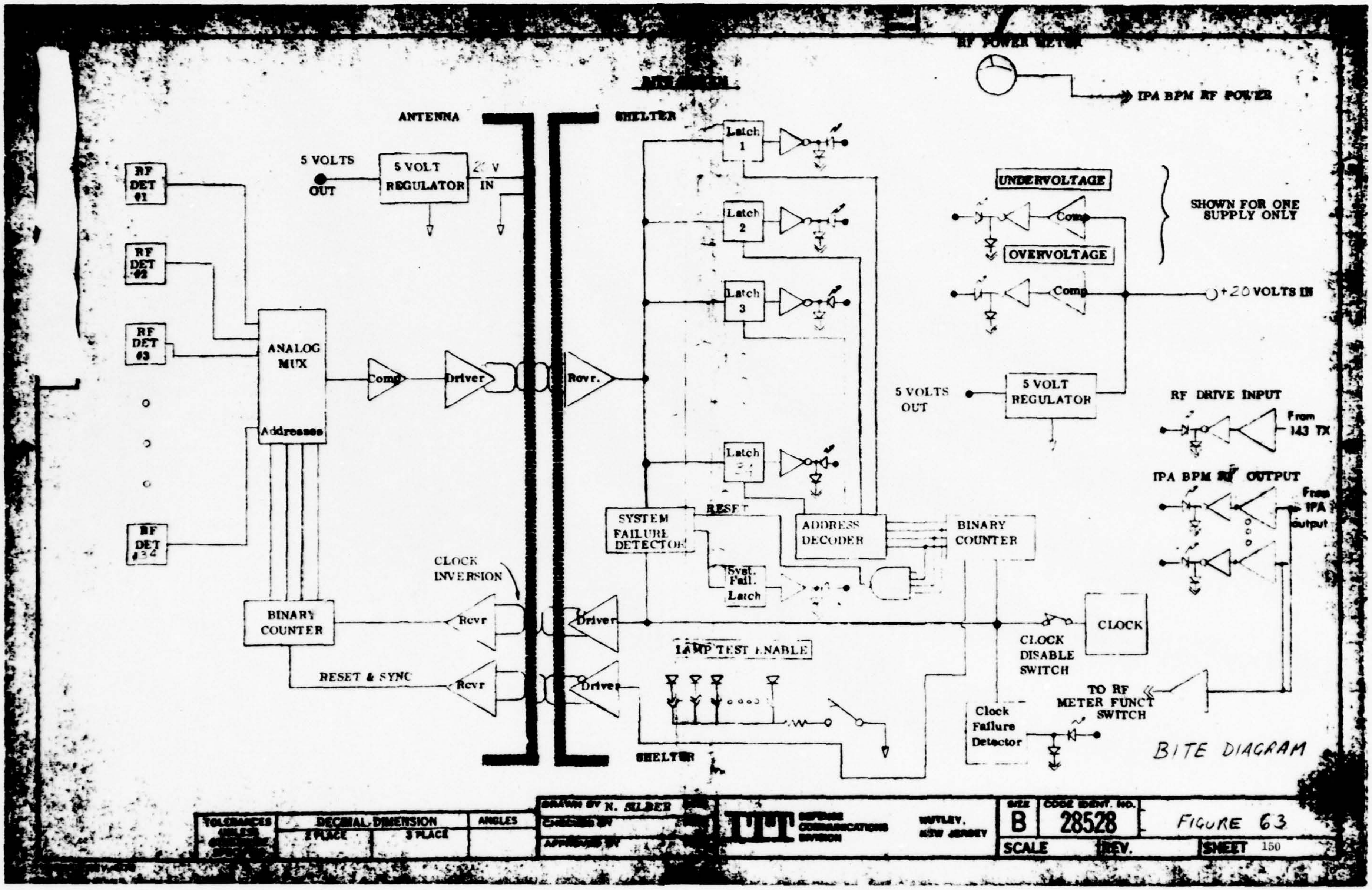
During normal operation of the Phased Array System, the RF output of each BPM is sampled and its status displayed via a control panel red LED. For normal operation the LED is off. In addition to an indication for each individual BPM, a monitor for the overall system failure status is provided. This consists of a red LED which is normally off when fewer than 9 BPMs fail. Computer analysis has shown that the system ERP will be degraded by $\leq$ 3 dB when fewer than 9 BPMs fail. (Graceful Degradation)

The power supplies for the IPA and Antenna Matrix BPM's would be provided with over and under voltage monitors which will show red to indicate when the voltage output exceeds the specified limits.

Detailed Description

Each BPM's RF power will be detected by a zero bias Schottky detector diode at the coupled output port of the final combiner hybrid (Part of BPM).

This eliminates the need to add an additional coupler to detect RF power, and therefore, cuts RF losses by about 0.1 dB per BPM. This method of detection was selected as the most reliable indication of normal operation. Other methods were considered, such as sensing the DC bias current or sensing transistor temperature. These were rejected on the basis that there were failure modes that could give erroneous indications, or worse, go unnoticed.



ANTENNA
SHELTER
RF POWER METER
IPA BPM RF POWER
RF DET #1
RF DET #2
RF DET #3
RF DET #34
5 VOLTS OUT
5 VOLT REGULATOR
20 V IN
ANALOG MUX
Addresses
Comp
Driver
Rcvr.
BINARY COUNTER
CLOCK INVERSION
Rcvr
RESET & SYNC
Latch 1
Latch 2
Latch 3
Latch 34
RESET
SYSTEM FAILURE DETECTOR
Syst. Fail. Latch
ADDRESS DECODER
BINARY COUNTER
LAMP TEST ENABLE
UNDERVOLTAGE
OVERVOLTAGE
SHOWN FOR ONE SUPPLY ONLY
+20 VOLTS IN
5 VOLTS OUT
5 VOLT REGULATOR
RF DRIVE INPUT
From 143 TX
IPA BPM RF OUTPUT
From IPA output
CLOCK
CLOCK DISABLE SWITCH
Clock Failure Detector
TO RF METER FUNCT SWITCH
BITE DIAGRAM
DRAWN BY N. SILBER
CHECKED BY
APPROVED BY
TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL DIMENSION
2 PLACE
3 PLACE
ANGLES
ITT DEFENSE COMMUNICATIONS DIVISION
NUTLEY, NEW JERSEY
SIZE B
CODE IDENT. NO. 28528
FIGURE 63
SCALE
REV.
SHEET 150

Since each BPM has two final stage transistors, it is conceivable that only one could fail. For this condition RF power would drop 6 dB. However, this partial failure condition has not been included in the computer analysis of ERP degradation vs. BPM failure. Thus the limit of 9 BPM failures is conservative.

Each of the 34 BPM detector outputs will feed analog multiplexer IC. Each multiplexer is a 16 channel MOS device that, upon accessing a specific address via a separate 4-bit binary coded input, will cause this input to appear at its output terminal. This multiplexed signal drives a threshold comparator. The BPM status voltage (detector output) drives the positive input of the comparator. The negative input of this device is biased at a slightly lower voltage (Reference). Normal operation will provide a true ("1") output from the comparator.

A failed or partially failed BPM will provide a detected voltage below this threshold. Thus, the comparator output will be a logic "o". Failure of the DC bias supply or a circuit interruption (wire break) will also indicate failure. This is a desirable 'failsafe' design.

This arrangement allows the high input impedance of the comparator to be used, decreasing the possibility of loading on the BPM detector diodes. From the comparator, the signal goes to a line driver. This line driver transmits the status bit stream on a balanced line to the control cabinet. This scheme provides superior noise immunity. The multiplexed signal is distributed from the balanced line receiver to IC latches for decoding. The demultiplexing is accomplished as follows: the Bite clock drives a binary counter which, in turn, steps the addresses of a decoder. This device 'enables' each latch one at a time, causing its output to agree with the signal at its input. The latch is not enabled until the middle of the current clock cycle. This allows the multiplexed bit stream to 'settle down' prior to information storage. This will eliminate false failure indications in the status circuitry. These latches are D-type flip flops which will change their state on a positive clock edge.

Any further change in the flop input, possibly caused by noise in the environment, will have no effect, even while it is in the enabled state, until the flip flop is sampled again. Each latch drives a buffer which, in turn, drives a red LED. This LED will normally be OFF. The control cabinet front panel LED layout could reflect the actual placement of each amplifier in the array facilitating fault location.

The multiplexed bit stream is also fed into a programmable counter which is enabled as each latch is enabled. If, during its enable period, a "high" input occurs (indicating that that particular amplifier is functional), no count is initiated. If a "low" occurs, however, the counter steps. When the count reaches 9 - the predetermined system failure point - the "overall system" failure indicator lights. It will remain lit until the operator affects a repair. No other reset action is required, since the system counter is automatically reset preceeding each new sampling cycle.

In addition to monitoring the amplifiers, all power supplies are monitored by a pair of comparators. These comparators allow a window for acceptable operation. If a power supply were to exceed the upper or fall below the lower limits, the respective indicators would light.

Other indicators incorporated in the Bite system include an RF Drive LED which indicates application of RF drive power to the system.

The IPA RF output power is read on the panel meter when the meter select switch is in IPA position. This signal is generated by summing the detector outputs of each IPA BPMs via a summing amplifier. These detectors also drive front panel status indicators (LED) via threshold comparators.

The Bite Clock indicator is connected to a monostable multivibrator, or "1-shot". If this Bite clock or square wave generator were to fail, the present status of the system would be frozen, and no new updates would occur. Each

time the clock goes high, it retriggers the one-shot. The period of the one-shot is slightly longer than that of the clock. The clock in effect continuously prevents the one-shot from completing its cycle. If, however, the clock fails, then the one-shot would finish its timing cycle and present an output state change. This output is the "Bite clock" failure indicator.

A lamp test function is provided. Connected to each panel LED is the anode of a diode (part of an IC diode array). All the cathodes of these diodes are common and are grounded momentarily by the "lamp test" switch. This switch is necessary since normal operation for the LED's if OFF. This provides an easy method of determining that all LEDs are functional. With the monitors operating in a normally OFF mode, Bite circuit power drain is reduced dramatically, as the LED's by far consume the greatest current. CMOS IC are extensively used in the Bite system. Current consumption for these devices is in the nanoamp range. Another advantage to CMOS is its ability to operate from varying power supply levels. Thus, their bias can be increased to provide noise margin.

Finally with the advent of microprocessors qualified for Military application a very significant portion of this BITE circuitry could be accomplished in software, further reducing IC chip count.

BITE CIRCUIT PACKAGE

The BITE circuitry is divided into two parts. One circuit board is located at the antenna, and the second circuit board is located in the Control Cabinet.

III G. COSTS

In developing the systems approach for a 1 kw antenna amplifier, cost is a major factor. This section will address the production costs of a 1 kw solid state array.

The 1 kw Solid State Phased Array Antenna Amplifier must be cost competitive with existing Klystron tube systems such as the AN/GRC-143 AM-6090 High Power Amplifier and 10 foot parabolic dish antenna (AN/TRA-37). Thus the starting point for this analysis will be the material costs for the AM-6090 HPA & AN/TRA-37 antenna. The current material costs for the Klystron tube HPA and antenna is approximately $50 K at acquisition, for quantities of 10 units.

The comparable Phased Array System as proposed in Section III of this report will consist of the following items with the estimated percentage of the total costs:

A. Control cabinet including DC power supplies, built in test equipment (BITE) and operator controls — 20%

B. Antenna feed system including the printed antenna laminates, waveguide, power dividers, attenuators, baluns — 25%

C. Mechanical structure including 1083 mast, Honeycomb ground plane, fasteners, inserts, stiffener, yoke — 10%

D. Basic Power Modules (BPM) including Intermediate Power Amplifier — 45%

Computing the costs of each item above, we have:

A	20%	x	50K	=	10K
B	25%	x	50K	=	12.5K
C	10%	x	50K	=	5k
D	45%	x	50K	=	22.5K
	100%	x	50K	=	50K

The production costs of the solid state antenna amplifier concept is primarily driven by the cost of transistors (GaAsFET or Bipolar). This is due to the quantity of devices involved per system and the fact that the required devices have yet to reach the full scale production phase.

For Item D above - BPM and IPA - the 1 kw system requires 34 antenna BPM, 4 IPA BPM, spare(1), and 1 IPA driver. Based upon the scale model development, the IPA Driver is one-half the cost of a BPM. We have:

$ 22.5K/39.5 = $ 570 per BPM.

This price has been derived by comparison to a Klystron tube system of quantity 10. The comparable number of BPM's is 39 units/system x10 systems = 390 BPM's.

To derive the required cost for the transistors, a breakdown of the BPM is required.

Using the scale model BPM as a guide, the parts breakdown expressed as a percentage is as follows:

BPM	
2 Driver Stage Transistors	20%
2 Final Stage Transistors	60%
Isolator	7%
Substrates*, Chassis, and Heat Sink	5%
Components (RF loads, RF, and DC Connectors, etc.	8%
	100%

* Other than Alumina

The transistor account for 80% of the BPM cost. Thus, a target price for the devices is:

Driver Stage Devices (2)	20% x \$570 = \$114	\$57 each
Final Stage Devices (2)	60% x \$570 = \$342	\$171 each
	80% x \$570 = \$456	

The above price \$57/\$171 are for quantities of 39 x 2 x 10 = 780 pieces of each type (Driver/Final) for 10 systems.

Using industry data for cost reduction for increased quantity, for 100 systems requiring 7800 pieces of each device, the cost per device would be less than 40% of the above costs.

	10 Systems (780 each)	100 Systems (7800 each)
Driver Stage Device	\$57 each	\$23 each
Final Stage Device	\$171 each	\$70 each
BPM	\$570 each	\$230 each

Thus with these cost targets established, an assessment of device availability can be made. The first realization one must make is that no transistor manufacturer is currently producing 5 GHz, 17 W devices in volume. These devices have been demonstrated in the laboratory at NEC and BELL laboratory. Based on previous history, the lead time from the laboratory to production takes from 6 to 18 months.

Second, at introduction to the market place, the per unit cost will be high, much higher than the \$171 price for quantities of 780 established above. Based upon price trends for power microwave devices at introduction, the unit price may be as high as \$1000 in small quantity. Typically, the price break for quantities of 1000 would be 1/2 the unit price. As the device matures and more importantly as competition among manufacturers develops, the unit/quantity pricing drops significantly.

Manufacturers of Microwave transistors supplied price trends and unit prices for various quantities of currently available devices. Using this as a basis, the curves of Figure 64 were developed.

The first 3 curves show the trend and from these the 4th curve (17 w device) was constructed. As more manufacturers develop the higher power parts, the supply becomes greater, competition increases, interests in parts increases (demand) so that the flattening out of curve 2 may not occur. Thus the eventual price for the 17 w device could fall to $400 or less after 24 months. These prices are for one device in small quantity. For quantities of 780 or greater, the price reduction would be approximately half. Thus after 24 months, a 17 w device would be available in quantity for $200 or less, very nearly approaching the target price of $171. Of course, these are projections but the technology of power GaAsFETs is rapidly emerging with no less than a dozen comapnies actively developing a power GaAs FET line. Thus with this increased competition, supply and demand, the costs of devices will rapidly drop, providing the devices at a suitably low cost to make a 1 kw Solid State Phased Array Antenna feasible.

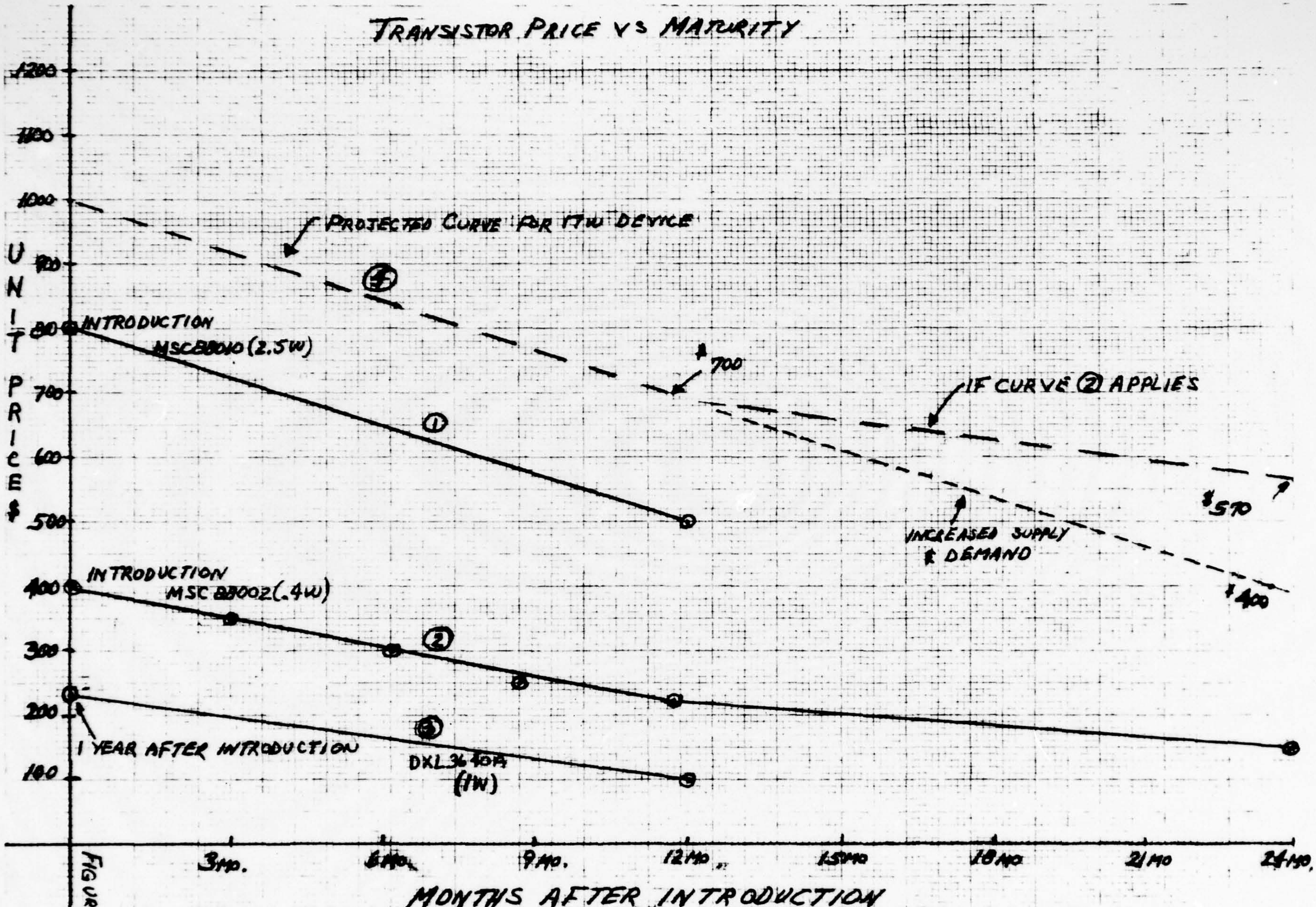

TRANSISTOR PRICE VS MATURITY
PROJECTED CURVE FOR 17W DEVICE
INTRODUCTION
MSC88010 (2.5W)
$700
IF CURVE 2 APPLIES
INCREASED SUPPLY & DEMAND
$570
$400
INTRODUCTION
MSC 82002 (.4W)
1 YEAR AFTER INTRODUCTION
DXL3640A (1W)
UNIT PRICE $
1200
1100
1000
900
800
700
600
500
400
300
200
100
3MO.
6MO.
9MO.
12MO.
15MO
18MO
21MO
24MO.
MONTHS AFTER INTRODUCTION

FIGURE 64

IV SUMMARY

The development of the scale model Phased Array Antenna Amplifier has shown that the concept of spatial addition of many lower power modules is feasible for a duplex communications system. The analysis and test of the scale model and cost comparison to existing Klystron systems indicate that a competitive full scale 1 kw solid state system is attainable within a two year period.

In addition to production costs, several other factors affect the favorable comparison of a solid state phased array system to the Klystron tube system. These are:

Reliability: The solid state system will be more reliable than a Klystron tube system due to its graceful degradation feature of many lower power modules spatially combined. Additionally, a regular maintainance schedule could extend the period between communication outages by replacing failed BPM (Basic Power Module) prior to a 3 dB loss in ERP. Additionally, the absence of high voltage, eliminates the dangers presented to operators and maintainance personnel. Finally an aspect generally overlooked in development phases of a concept, is life cycle costs. Klystron tubes are generally guaranteed for 1000 hour operation or 1 year shelf life. Thus sparing tubes at a depot implies 1) large expenditure per tube (~$10k each), 2) a possibility that spared tubes may go "gassy" and if reclaimed (by applying beam voltage at increasing levels over a period of time) may take a full day prior to resumption of communications, 3) even if reclaimed, a tube may not provide the 1000 hours operating life prior to a need to replace it. Comparing this to solid state hermetically sealed devices, with essentially unlimited shelf life, lower unit costs, inherent ruggedness, quick replacement time, and sparing at the equipment level (due to small, lightweight packaging), equipment outage for replacement could be less than an hour.

Size and Weight: The control cabinet portion of the 1 kw system will be no heavier or larger than the comparable Klystron HPA cabinet. Additionally, the thermal characteristics should be less stringent since the greater quantity of RF amplifiers (BPM) are located on the antenna structure. This lower operating temperature would significantly add to the MTBF of the control cabinet components.

The antenna structure for the 1 kw solid state system will be heavier than its counterpart AN/TRA-37. However, the current 1083 mast is sufficient for both systems. Because of the modular arrangement of the solid state antenna, erection time and storage needs will be comparable to the parabolic dish antenna.

Efficiency: With the continued development of high power transistors, the AC-RF efficiency will rapidly approach the Klystron tube system. Transistor efficiency of 35% will provide comparable performance to the Klystron tube system. Additionally, as seen at lower frequencies, transistor devices evolved with >60% efficiency at "L" Band and a 35% efficiency at 'C' Band is not a theoretical limit.

Thus, the efficiency of the solid state system will improve with device development eventually surpassing the Klystron tube system.

Broadband Operation: As demonstrated on the scale model system, full band (4.4 - 5.0 GHz) performance was achieved in the Basic Power Modules (BPM) without tuning. The 1 kw solid state system will also comply with the non-tunable requirement.

Duplex Operation - Noise Characteristics: The scale model system demonstrated the duplex operation of an AN/GRC-143 transmitter and receiver with no measureable degradation to receiver noise threshold. This performance is related to the transistor noise power, receive-transmit polarization isolation and antenna amplifier (BPM) gain. The 1 kw system addressed this parameter and concluded

that this performance is achieveable if comparable noise power is obtainable with the higher power transistors.

Thus, all of the key parameters required for a successful full scale 1 kw Phased Array Antenna Amplifier have either been demonstrated at the scale model evaluation or have been shown to be compliant with progressing technology.

APPENDIX A

TEST PLAN

REQUIRED TESTS & DATA

PHASED ARRAY ANTENNA AMPLIFIER

<u>TEST PLAN</u>

DAAB-07-C-77-0146

TP1

TABLE OF CONTENTS

LIST OF FIGURES

PHASED ARRAY ANTENNA AMPLIFIER

TEST EQUIPMENT

ITEM	MODEL*
RF Sweeper	HP 8690 A
Plug-in	HP H03-8693B
Attenuator	
TWT	Servo 2130
Circulator	
Load	
LPF	
Coupler #1	NARDA 3004-20
Attenuator	
Counter	HP 5340A
Coupler 2	NARDA 3044-20
Wavemeter	HP 637A
Coupler 3	Wavecom L910-13
Attenuator	
Attenuator	
Power Detector	Booton 41
Power Meter	Booton 42B
Circulator	
Power Supply	LAMBDA LK-343A
Power Supply	HP 6102A
Voltmeter	HP 3430A
Selective Voltmeter	Wandel Goltermann TFPM-43

* Or Equivalent

TP4

ITEM	MODEL*
Attenuator	NARDA 766-20
Attenuator	NARDA 777C-10
Thermistor	HP 478 A
Power Meter	HP 431 C
Detector	HP 423 A
Oscilloscope	TEK 545 A
Plug-in	TEK CA

TPS

3.4.1.1 <u>Size</u> Cross sectional area not to exceed 10 square feet.

Test Procedure: Cross sectional area of the antenna array will be calculated from:

$A = W \times H$

Where W = Width of the array, <u>inside frame</u> W = 3.16 ft

H = Height of the array, <u>inside frame</u> H = 3.16 ft

$A = W \times H$

$A = \underline{3.16'} \times \underline{3.16'} = \underline{9.96}$ SQ FT

Limit 10 square feet (1440 sq. inches)

TP6

3.4.1.2 <u>Temperature Independent Operation</u>. The phased array antenna amplifier shall be designed to meet all specifications from $-65^{o}F$ (no solar loading) to $+125^{o}F$ (with 360 $BTU/ft^2/hr$ solar loading).

The scale model Phased Array Antenna Amplifier has been designed to meet all specifications over a $-65^{o}F$ to $+125^{o}F$ with 360 $BTU/ft^2/hr$ solar loading. As presented in the Preliminary Design Plan, for an ambient temperature of $+125^{o}F$ with solar loading, the worst case temperature is $+160^{o}F$ ($71^{o}C$). Equipment built by ITT DCD for military deployment is tested over this $-65^{o}F$ to $+160^{o}F$ temperature range. The critical components are the GaAsFET's. Typical operating conditions for these components are P_{DC} = 9 watts, Pout = 2.5 w and $R_{TH} = 10^{o}$ C/W. This results in an increase in transistor channel temperature of $65^{o}C$ above ambient. This number is within the recommended channel temperature for GaAsFET's over the full ambient range.

To ease cost and delivery problems, some commercial grade components were used in the system. Full military grade versions of the same components are available, however, for future systems.

TP 7

3.4.1.3 **Weight.** The weight of the phased array antenna amplifier shall be kept to a minimum.

Test Procedure:

The weight of the final Phased Array Antenna complete with all amplifier modules, power splitters, and cables will be measured and recorded.

Control Cabinet	98	lb
Antenna Array	120	lb
Interconnect Cables	26	lb
Total	244	lb

Limit: Minimum

TP 8

3.4.1.4 Structural Interface - The Phased Array Antenna will include the necessary hardware to mount the antenna on an AB-216 tower.

Hardware to mount the antenna to the AB-216 tower is included in the antenna design. Included in the design are several safety features which secure the antenna assembly during alignment.

✓ (ITT) ________ (COTR) COMPLIES (V)

3.4.1.5 Input/Output Connectors - Input connector to the Phased Array Antenna Amplifier shall be a coaxial type N. Output connector to the AN/GRC-143 receiver shall be WR-187 with UG/149 flange.

The input connector to the Phased Array Antenna Amplifier is a type N female connector mounted to the top of the control cabinet.

The output of the receiver array is WR-187 waveguide with UG/149 flange.

Input Conn ✓ Complies (V)

Receive Conn ✓ Complies (V)

TP9A

3.4.1.6 Cooling - All cooling mechanisms shall be integral to the antenna structure with the cooling technique limited to air cooling methods.

Thermal analysis on the antenna structure has indicated that convection cooling is adequate to cool the antenna mounted amplifier modules.*

A fan is included in the control cabinet to cool the IPA module and the two power supplies.

*This analysis, included in the Preliminary Design Plan, was completed for 12 antenna mounted BPM. This analysis is more conservative in view of the reduced number of antenna BPM and GaAsFET devices. Therefore, at elevated ambient temperature, the natural convection cooling is adequate to maintain the GaAsFET channel temperature below the maximum permissable.

Cooling Technique ✓ Complies (V)

TP 10A

3.4.1.7 Mechanical Positioning - Mechanical positioning aids integral to the antenna atructure shall provide 360° (±.5° Accuracy) azimuth and ±5° (± 0.2° Accuracy) elevation positioning.

Azimuth and elevation positioning aids are included in the antenna structure. Azimuth positioning is obtained by loosening a lock bolt and rotating the antenna around the vertical member of the AB-216 tower. Total azimuth range is ±135° per corner. The required 360° range is obtained by moving the antenna structure to the other corners of the AB-216 tower. This is a continuous adjustment mechanism consistent with the ±0.5° accuracy.

Attached to the AB-216 tower vertical member is a stop collar. The antenna structure rests on this collar. The collar will be marked in .5° increments. Movement of the antenna structure via the positioner will rotate the azimuth indicator mark on the positioner with respect to the collar marking. This will provide the .5° resolution.

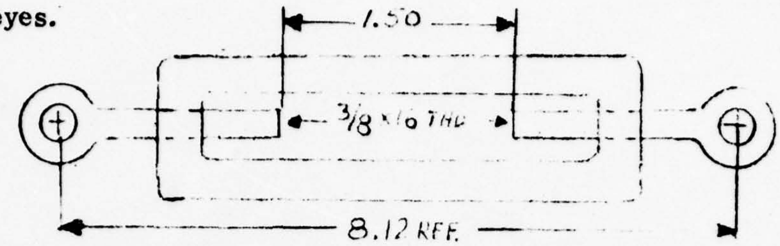
Elevation positioning is provided with two turn-buckles. Calculations show that the required ±5° range can be obtained from 22 1/2 full rotations of the turn buckle. One half turn results in approximately 0.22°. See Figure 3.

Attached tothe upper antenna mount will be a level indicator with pointer. A scale, marked off with .2° increments, will be provided. Rotation of the level pointer to the desired elevation angle is accomplished by rotating the pointer to the desired elevation mark. The antenna elevation is then adjusted until the level indicator is again reading 'level.'

TP11A

3.4.1.7 Elevation Adjust of Positioner

1 - Initialize antenna to 0^{o} axis by extending turnbuckles to 1.50 inch separation of the threaded eyes.



2 - At the rate of .0175 inches/inch per degree (for small angles 0 to 6^{o}), 5^{o} operating over 15.8 inch radius requires 1.3825" contraction or expansion of the eye bolt tips. This is accomplished via revolutions of the turnbuckle at the rate of 8 full turns per 1 inch excursion thus eleven and a quarter turns will accomplish 5^{o} or 22 1/2 for full $\pm 5^{o}$ range.

3 - Translation per turns of the turnbuckle therefore produces the following elevation angle change:

1/8 turn (45^{o} revolution) = $.0555^{o}$
1/4 turn (90^{o} revolution) = $.1110^{o}$
1/2 turn (180^{o} revolution) = $.2220^{o}$
9/16 turn (203^{o} revolution) = $.25^{o}$
1 1/8 turns (406^{o} revolution) = $.50^{o}$
2 1/4 turns (810^{o} revolution) = 1.00^{o}

FIGURE 3

3.4.2 Electrical Characteristics

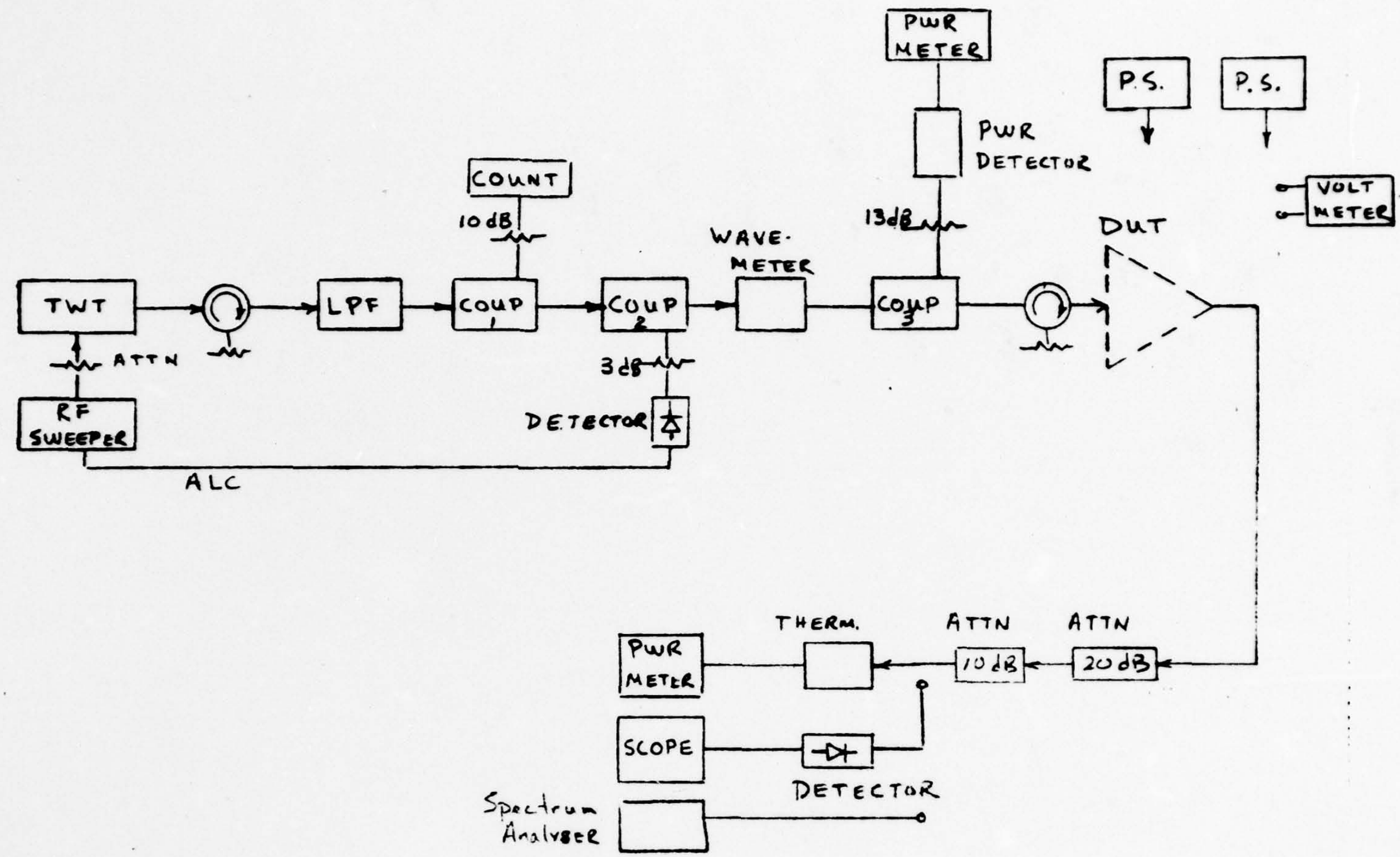
Unless otherwise stated, all electrical characteristics will be measured on the test set shown in Figure 1. A list of test equipment model numbers is included.

TP 13

ITT DEFENSE COMMUNICATIONS DIVISION

NUTLEY, NEW JERSEY

DRAWING NUM…R



PHASED ARRAY ANTENNA AMPLIFIER

AMPLIFIER TEST SET-UP

FIGURE 1

TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION		ANGLES
	2 PLACE	3 PLACE	

USED ON		CODE IDENT. NO.	DWG.
PREPARED BY	DATE	28528	A SIZE
CHECKED BY	DATE		

SHEET TP 14

D6216 A REV. 8/78

3.4.2.1 Antenna Matrix Gain and Beamwidth - (Setup per Figure 4)

Gain	30 dBi	Transmit and Receive
Beamwidth	5^{o}	Both planes

Test Procedure: The basic technique for measuring gain will be by comparison to a standard gain horn (SGH). In this technique, the SGH is substituted for the antenna under test in such a way that both range location and RF power are maintained as constants. Transmit and Receive arrays require different procedures.

A. The transmit array will be measured as a passive component by use of a calibrated 6:1 phased power combiner in place of the amplifiers. The gains measured by SGH comparison are corrected by addition of the combiner loss. Gain will be measured at a minimum of ten frequencies to provide a distribution of range error effects.

The receive array will be measured in a similar way except that the combiner, being integral to the receive array, requires no correction.

All gain tests will be performed on an outdoor, 1000 foot range which adequately provides a far field distance for the antenna size under test.

B. Beamwidth measurements will be performed both with and without the BPM's.

Passive tests of both Transmit and Receive arrays will be made at five frequencies and for two principal planes, horizontal and vertical. A 6:1 phased power combiner will be used on the transmit in place of the BPM's. The test method will consist of pattern recording of the output power of the antenna under test as it is rotated about a principal plane axis. The recorded data, power versus angle, is on a calibrated chart associated with a calibrated receiver and servo controlled pedestal. Beamwidth is read directly from chart.

Active testing of the transmit array will be done with all BPM's connected. Beamwidth will be measured by monitoring of unsynchronized transmitter power in the far field as the array is rotated.

TP15

The angular location of the pedestal will be recorded at each 3 dB below peak of the main lobe (maximum power point). The difference between angles is the beamwidth.

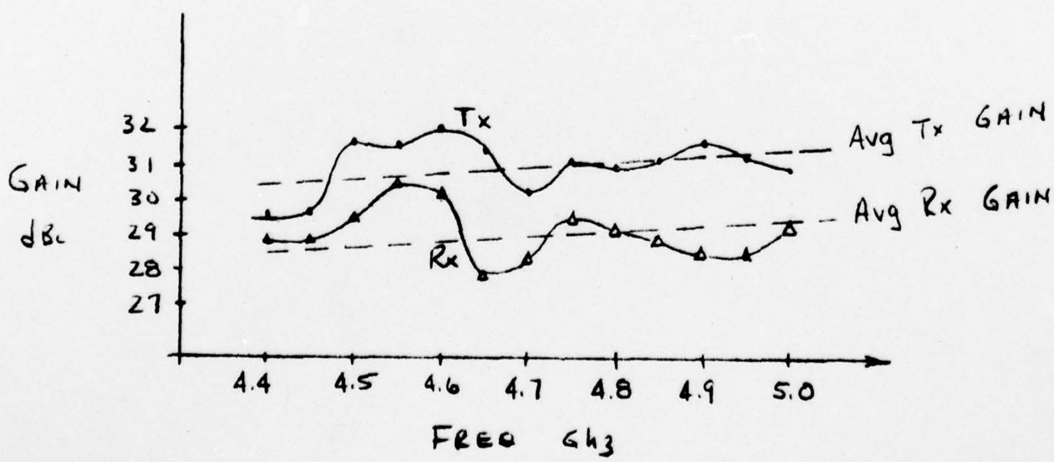
Active testing of the Receive array is not required.

All beamwidth tests will be performed on a far field, 1000 foot outdoor range.

TP 16

I] ANTENNA GAIN

FREQ (GHZ)	GAIN Tx	GAIN Rx
4.40	29.6 dBi	28.9 dBi
4.45	29.6	28.95
4.50	31.72	29.50
4.55	31.67	30.50
4.60	32.04	30.15
4.65	31.49	27.90
4.70	30.3	28.35
4.75	31.13	29.50
4.80	31.08	29.20
4.85	31.13	28.90
4.90	31.65	28.55
4.95	31.23	28.50
5.0	30.91	29.25



ITT DEFENSE COMMUNICATIONS DIVISION, NUTLEY, NEW JERSEY

DRAWING NUM

TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION 2 PLACE	3 PLACE	ANGLES	ANTENNA GAIN

USED ON	CODE IDENT. NO.	DWG. SIZE	
PREPARED BY DATE	28528	A	PHASED ARRAY
CHECKED BY DATE			SHEET TP16A

D8215 A REV. 6/73

II] ANTENNA BEAMWIDTH

A) PASSIVE TESTING / NO BPM'S

FREQ	Tx ARRAY VERT	Tx ARRAY HORIZ	Tx ARRAY INTER	Rx ARRAY VERT	Rx ARRAY HORIZ	Rx ARRAY INTER
4.40 Ghz	3.8°	3.8°	3.8°	3.8°	3.83°	3.83°
4.55	3.7°	3.7°	3.7°	3.7°	3.7°	3.90°
4.70	3.5°	3.5°	3.6°	3.5°	3.5°	3.75°
4.85	3.4°	3.4°	3.5°	3.5°	3.4°	3.60°
5.00	3.4°	3.3°	3.4°	3.3°	3.3°	3.50°

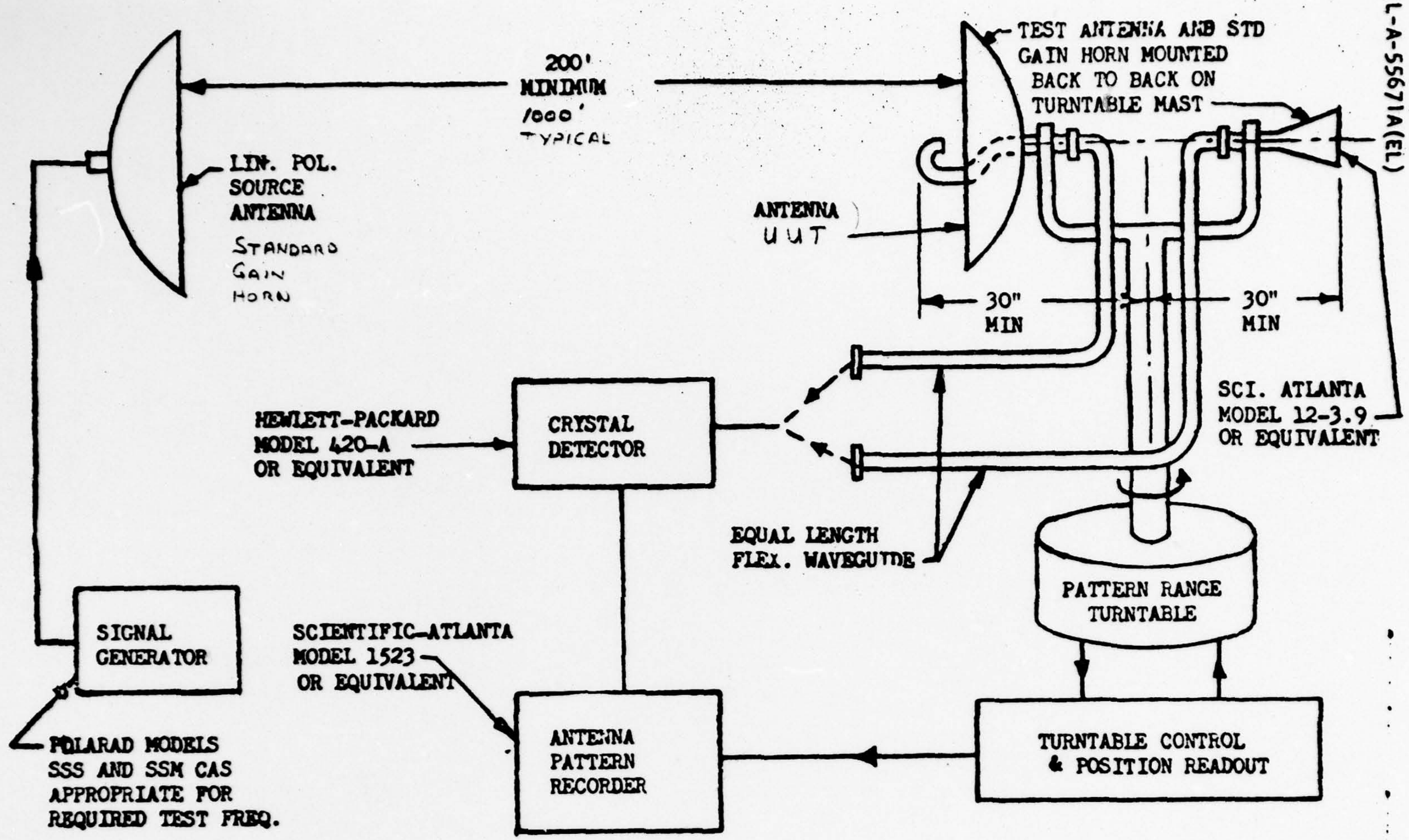
B) ACTIVE TESTING / Tx ARRAY WITH BPM'S

FREQ	Tx ARRAY VERT	Tx ARRAY HORIZ	Tx ARRAY INTER
4.40 Ghz	3.7°	3.7°	3.75°
4.55	3.8°	3.7°	3.75°
4.70	3.5°	3.6°	3.67°
4.85	3.4°	3.3°	3.6°
5.00	3.4°	3.3°	3.5°

1) VERTICAL POLARIZATION = E PLANE
HORIZONTAL POLARIZATION = H PLANE

TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION 2 PLACE	DECIMAL DIMENSION 3 PLACE	ANGLES	ANTENNA BEAMWIDTH
USED ON / PREPARED BY DATE / CHECKED BY DATE	CODE IDENT. NO. 28528		DWG. A SIZE	PHASED ARRAY
				SHEET TP16B

D5215 A REV. 5/73



BLOCK DIAGRAM FOR RADIATION PATTERN & GAIN TESTS

FIGURE 4

3.4.2.2 Duplex Operation - With receiver frequency separated 100 MHz from transmit frequency, overall effective receiver noise figure shall not be degraded more than 1.5 dB. This assumes a 5.5 dB Receiver Noise Figure. Thus, resultant receiver noise figure in the presence of colocated transmitter shall be less than 7 dB.

Test Procedure I

1. Noise power of each antenna mounted BPM will be measured as shown in Figure 2.

Noise Power (dBm/700 KHz)

$$Pn\ (dBm/Hz) = Pn\ (dBm/700\ KHz) - 10 \log (700\ KHz)$$
$$= Pn\ (dBm/700\ KHz) - 58.5\ dB.$$

2. Antenna Isolation (transmit array to receive array) will be measured on the Automatic Network Analyzer before the amplifiers are integrated into the system. To do this test, a transmit power splitter will be used. The loss of this power splitter will be measured and removed from the measured isolation.

3. Noise Figure Degradation will be calculated from :

$$NFD = 10 \log \left(1.41 \times 10^{-17} + 10^{\frac{(Pn\ (dBm/Hz) - I)}{10}}\right) + 168.5\ dB$$

where 1.41×10^{-17} = Receiver Noise Power (AN/GRC-143 Receiver - NF 5.5 dB) dBm/Hz

I = Isolation (dB)

NFD 0.89 dB Limit 1.5 dB

Test Procedure II

Connect equipment as shown in Figure 5. With Phased Array Antenna Amplifier turned off, plot a noise quieting curve. This is accomplished by connecting a sensitive receiver to the base band output of the AN/GRC-143 receiver and plotting base band level (dB) vs RF input level (dB). The input level is adjust by varying the RF attenuators. As receiver threshold is approached, the baseband signal (noise) will increase. Repeat this test with the Phased Array Antenna Amplifier turned on and plot the result on the same curve

TP 18 A

generated above. The difference (dB) between the two curves is degradation in receiver threshold.

0 dB Limit 1.5 dB Threshold Degradation

5.5 dB Receiver Noise Figure

5.5 Limit 7 dB Max Resultant Noise Figure

TEST PROCEDURE 1

I]. ISOLATION MEASUREMENTS - MEASURED FROM 6 Tx Baluns to common Receive port

BALUN	ISOLATION (MIN) & freq
T_1	32 dB at 4.4 Ghz
T_2	30 dB at 4.65 Ghz
T_3	32 dB at 4.58 Ghz
T_4	34 dB at 4.40 Ghz
T_5	34 dB at 4.55 Ghz
T_6	33 dB at 4.63 Ghz

$\Rightarrow$ WORST CASE ISOLATION = 30 dB

II] NOISE FIGURE DEGRADATION, NFD

$\rightarrow$ WORST CASE

$$NFD = 10 \log \left[1.41 \times 10^{-17} + \exp\left(\frac{P_n - I}{10} \right) \right] + 168.5 \text{ dB}$$

P_N = BPM Noise power = -144.9 dBm / Hz

I = Antenna Tx to Rx Isolation = 30 dB

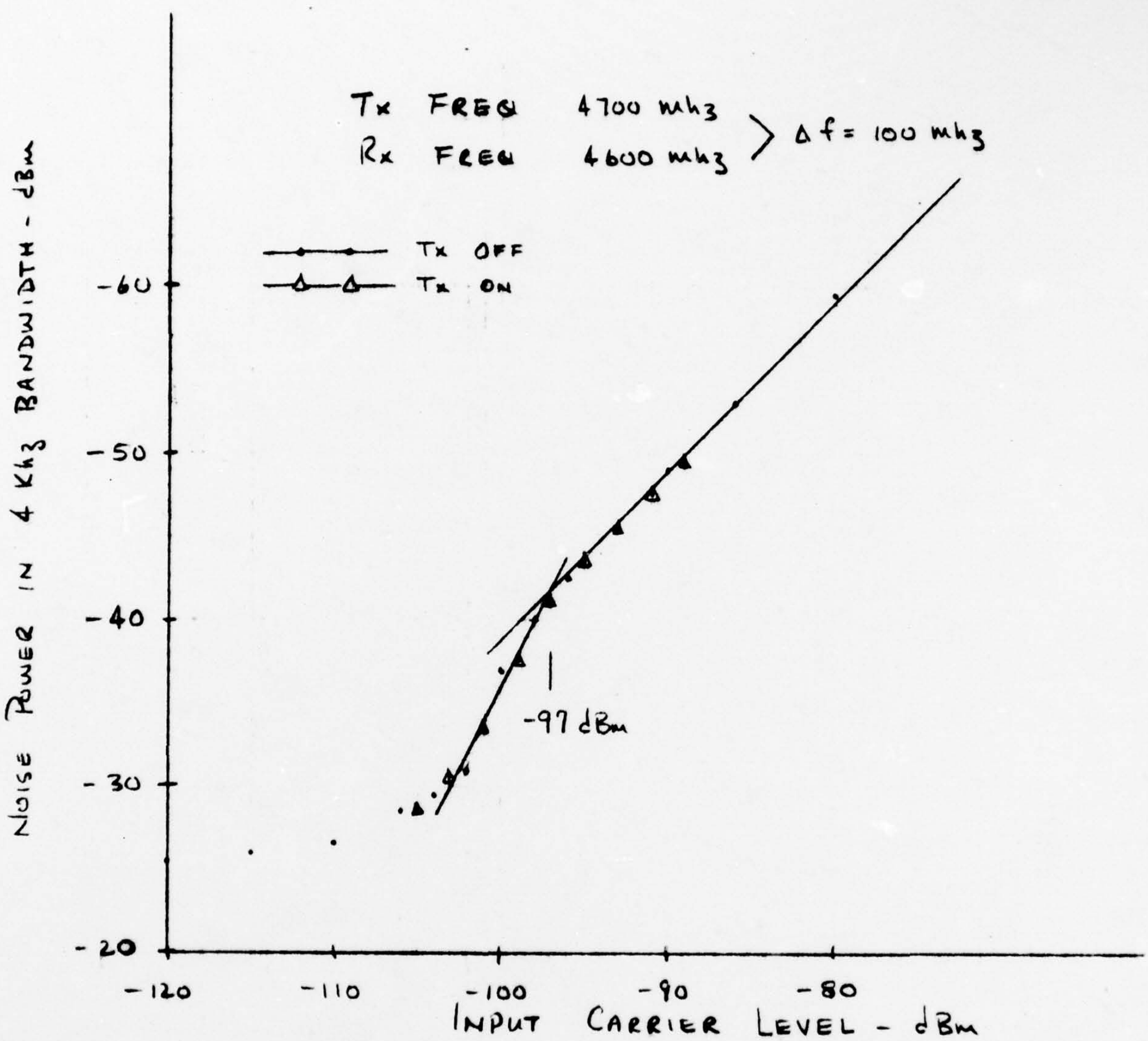
$\boxed{NFD = 0.89 \text{ dB}}$ WORST CASE WHEN RECEIVING AT 4.65 Ghz

$\rightarrow$ TYPICAL ISOLATION > 35 dB

$\Rightarrow$ NFD $\leq$ 0.3 dB

TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION 2 PLACE	3 PLACE	ANGLES	-NOISE FIGURE DEGRADATION-
USED ON	CODE IDENT. NO. 28528	DWG. A SIZE		PHASED ARRAY
PREPARED BY / DATE				
CHECKED BY / DATE				SHEET TP18C

TEST PROCEDURE 2 - NOISE QUIETING



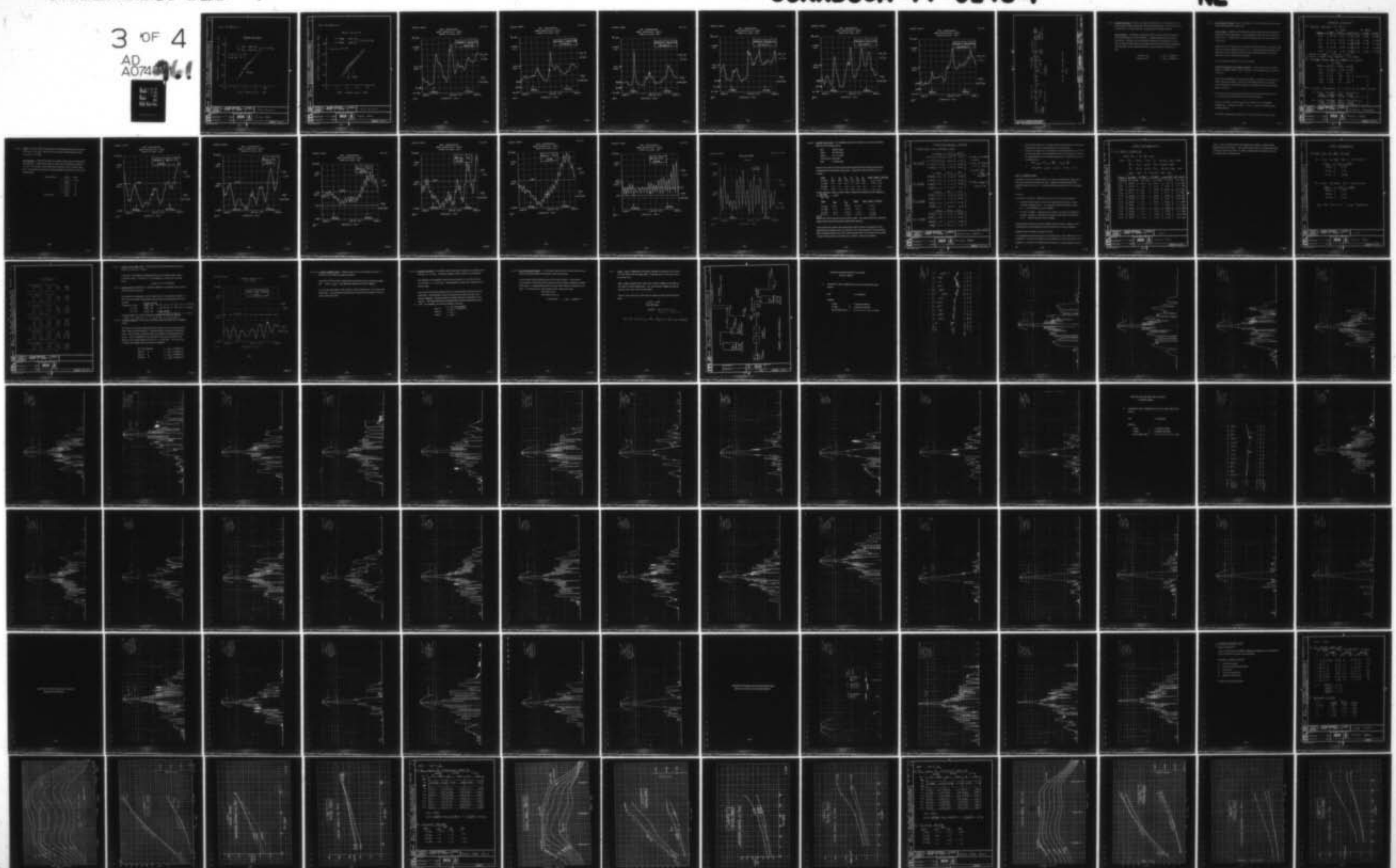
ITT DEFENSE COMMUNICATIONS DIVISION — NUTLEY, NEW JERSEY

TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION 2 PLACE	3 PLACE	ANGLES	NOISE QUIETING
USED ON	CODE IDENT. NO. 28528	DWG. A SIZE		PHASED ARRAY
PREPARED BY — DATE				
CHECKED BY — DATE				SHEET TP18D

D5215 A REV. 5/73

AD-A074 961 ITT DEFENSE COMMUNICATIONS DIV NUTLEY N J F/G 9/5
PHASED ARRAY ANTENNA AMPLIFIER EXPLORATORY DEVELOPMENT MODEL.(U)
AUG 79 P MUSCIANESI, J IRVINE, J RANGHELLI DAAB07-77-C-0146
UNCLASSIFIED CORADCOM-77-0146-F NL

3 OF 4
AD
A074961

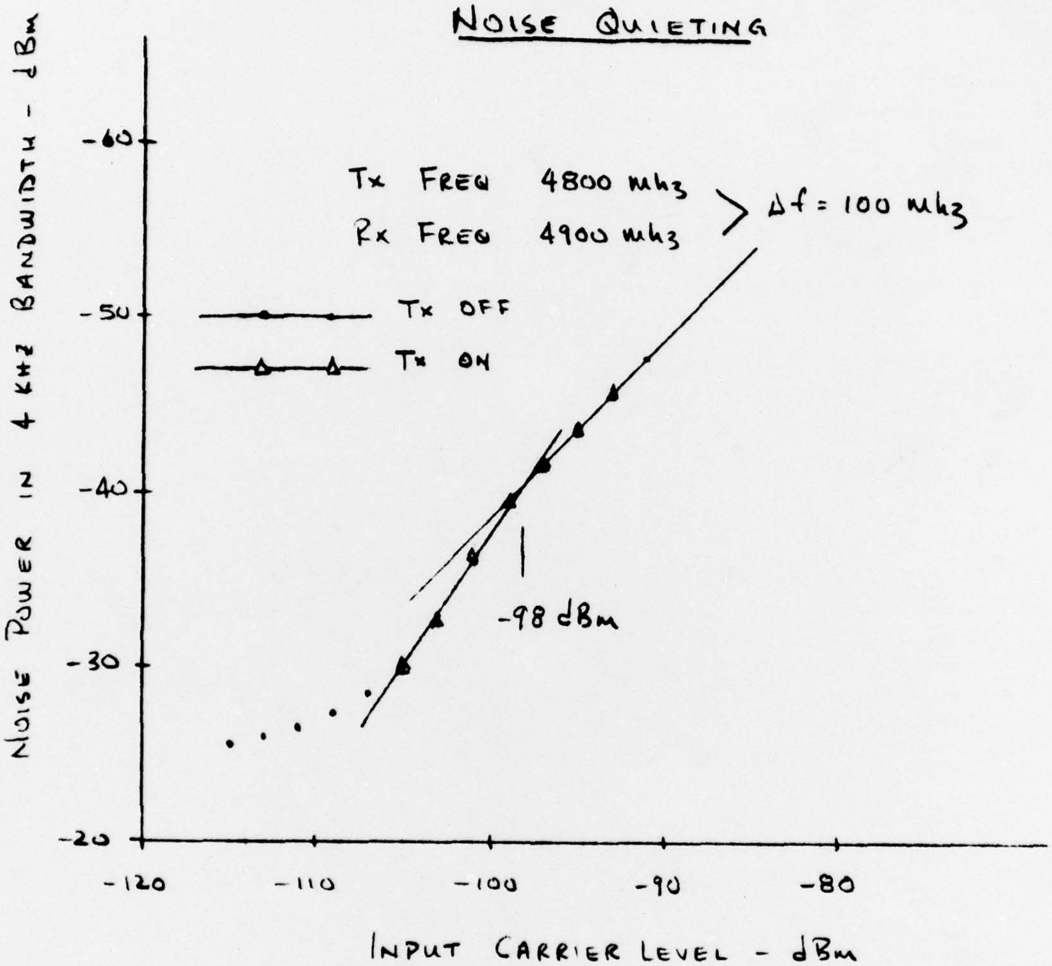


D
074

1.0 1.1 1.25 1.4 1.6 1.8 2.0 2.2 2.5 2.8 3.2 3.6 4.0

MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

TEST PROCEDURE 2

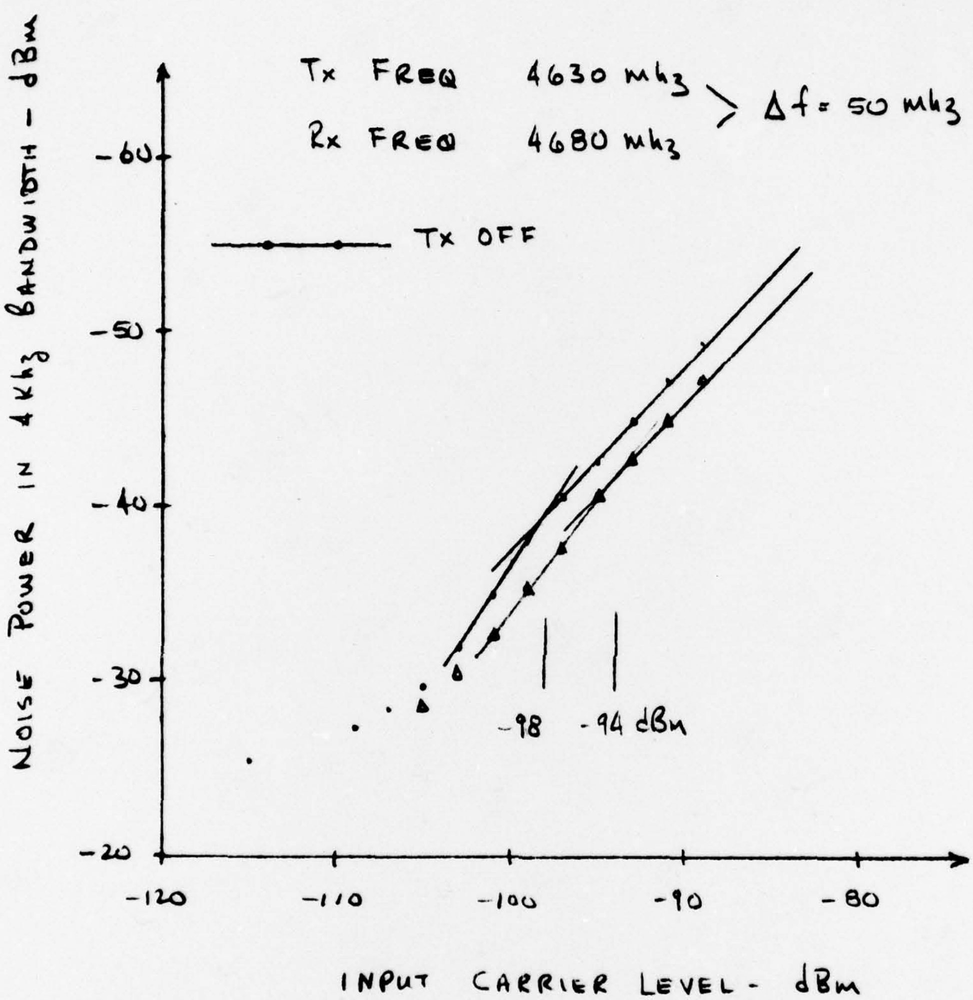


TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION 2 PLACE	3 PLACE	ANGLES	NOISE QUIETING

USED ON	CODE IDENT. NO.	DWG. SIZE	
PREPARED BY DATE	28528	A	PHASED ARRAY
CHECKED BY DATE			SHEET TP18E

TEST PROCEDURE 2

NOISE QUIETING



DRAWING NUM'

DEFENSE COMMUNICATIONS DIVISION NUTLEY, NEW JERSEY

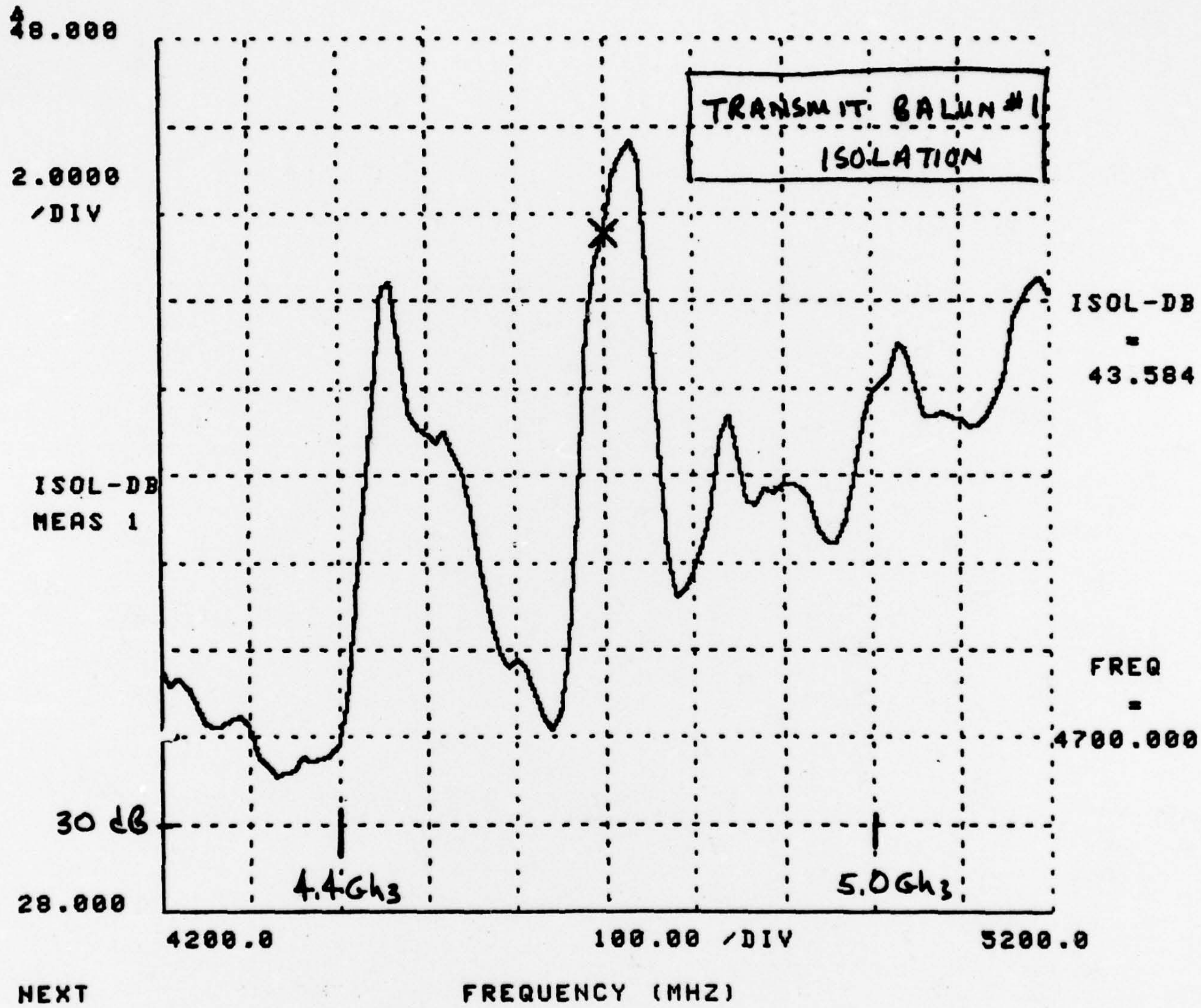
TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION		ANGLES	NOISE QUIETING
	2 PLACE	3 PLACE		

USED ON	CODE IDENT. NO.	DWG. SIZE	PHASED ARRAY
PREPARED BY — DATE	28528	A	
CHECKED BY — DATE			SHEET TP18F

D6215 A REV. 5/73

PHASED ARRAY 5-3-79

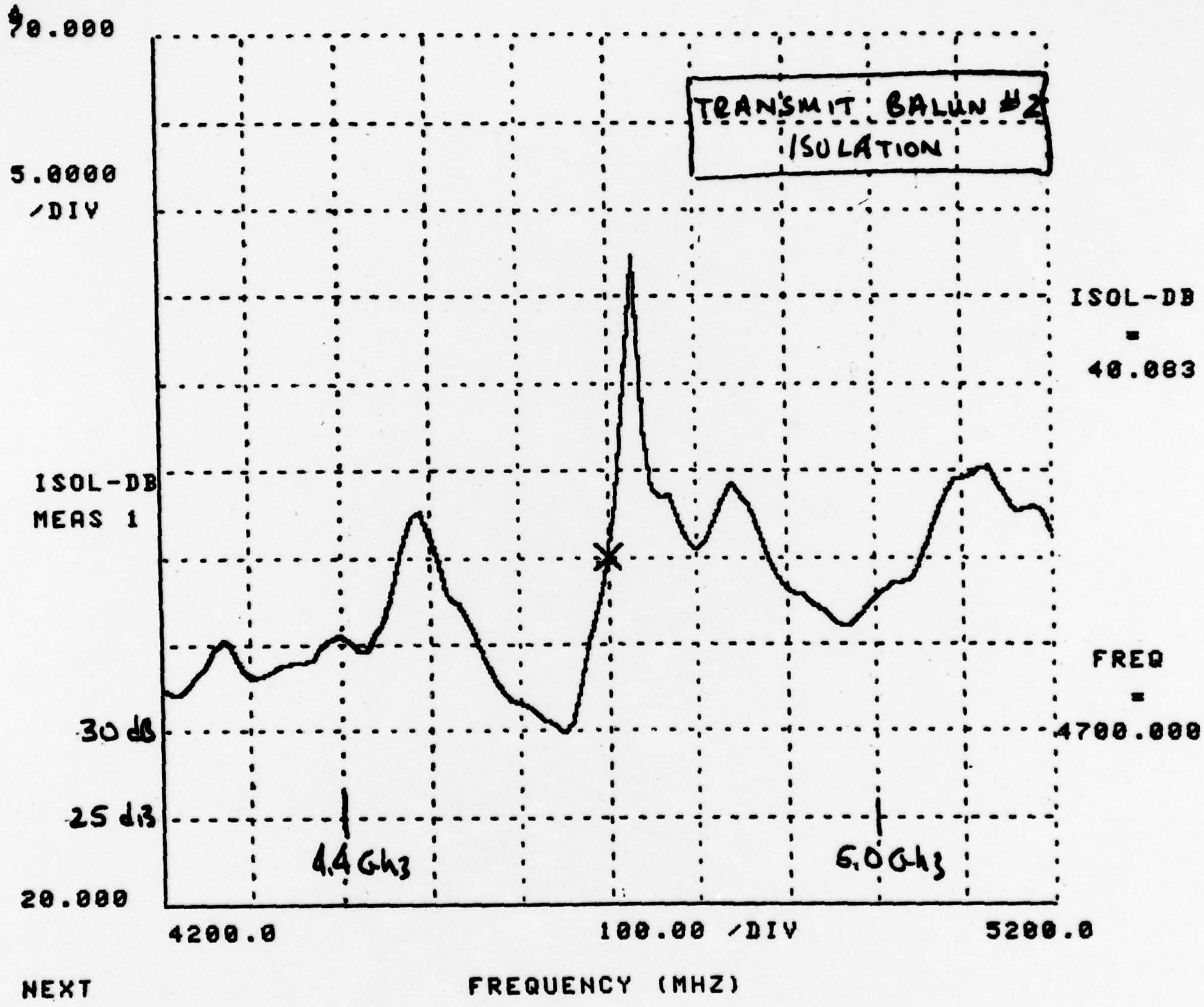
ANT. MEASUREMENT
WRAP AROUND/POLY SHEET
TRANS.#1/COMB. REC.



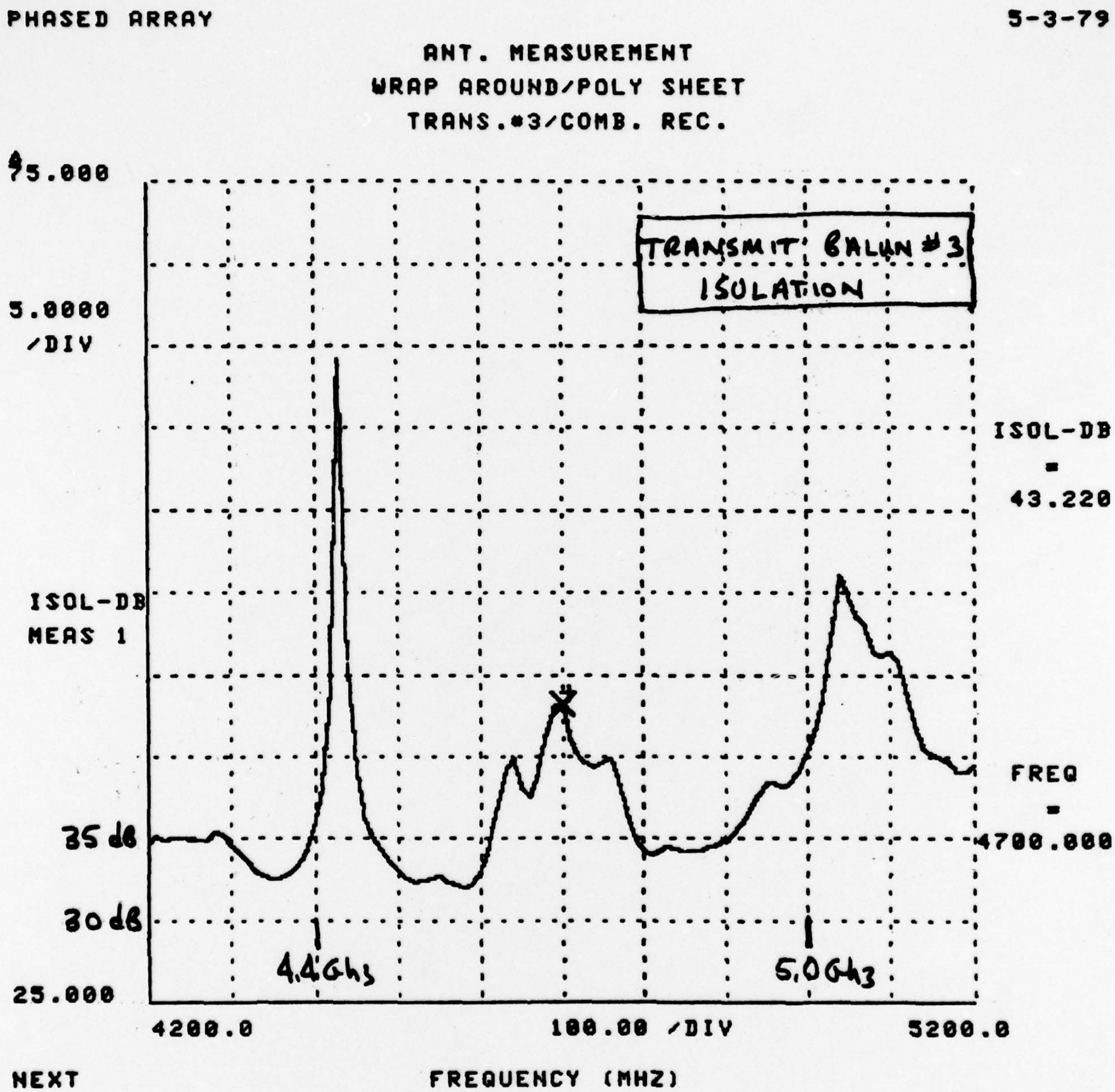
TP18G

PHASED ARRAY 5-3-79

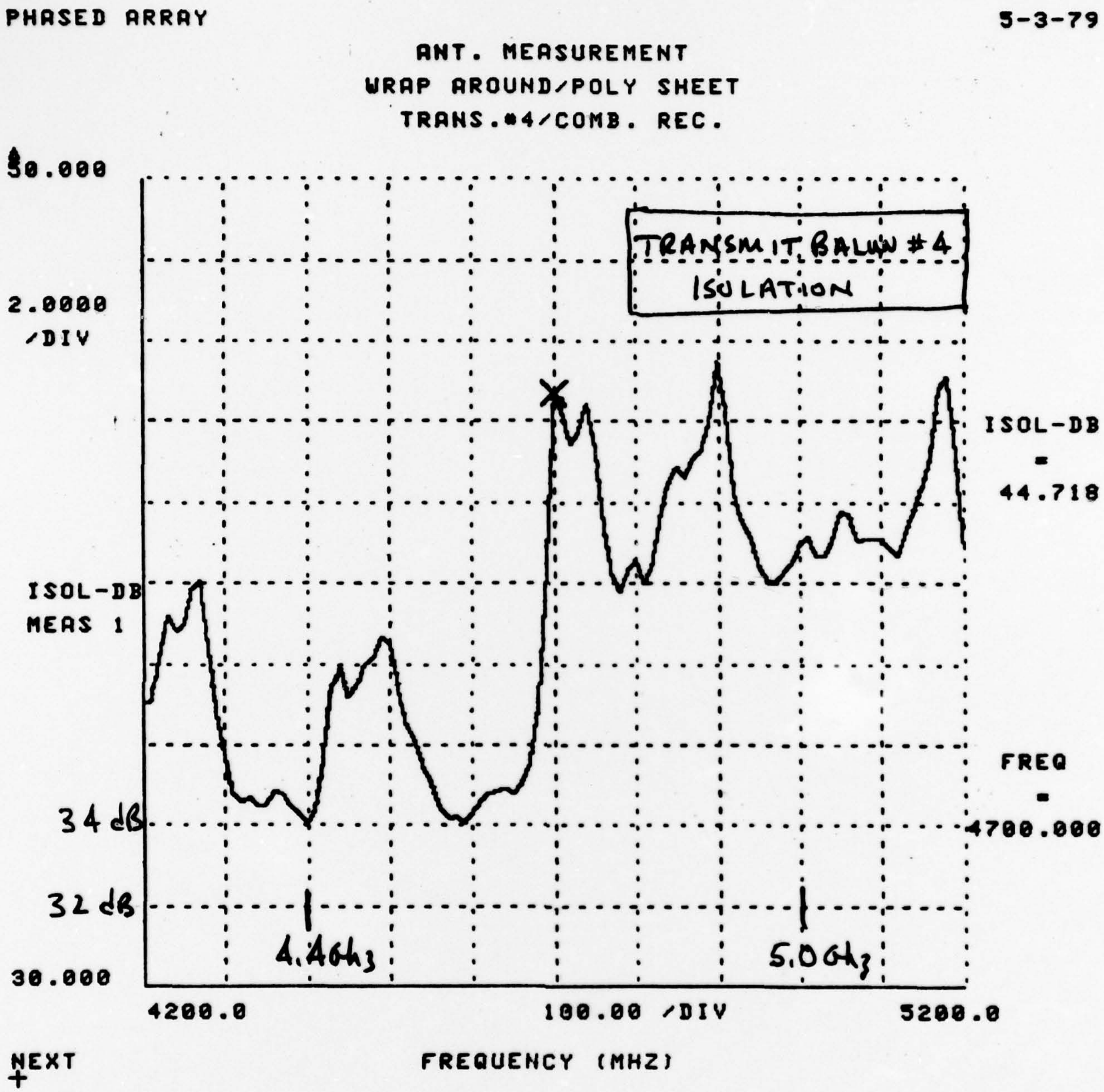
ANT. MEASUREMENT
WRAP AROUND/POLY SHEET
TRANS.#2/COMB. REC.



TP18H


PHASED ARRAY
5-3-79
ANT. MEASUREMENT
WRAP AROUND/POLY SHEET
TRANS.#3/COMB. REC.
45.000
TRANSMIT BALUN #3
ISOLATION
5.0000
/DIV
ISOL-DB
=
43.220
ISOL-DB
MEAS 1
FREQ
=
4700.000
35 dB
30 dB
4.4 Ghz
5.0 Ghz
25.000
4200.0
100.00 /DIV
5200.0
NEXT
FREQUENCY (MHZ)

TP18 I

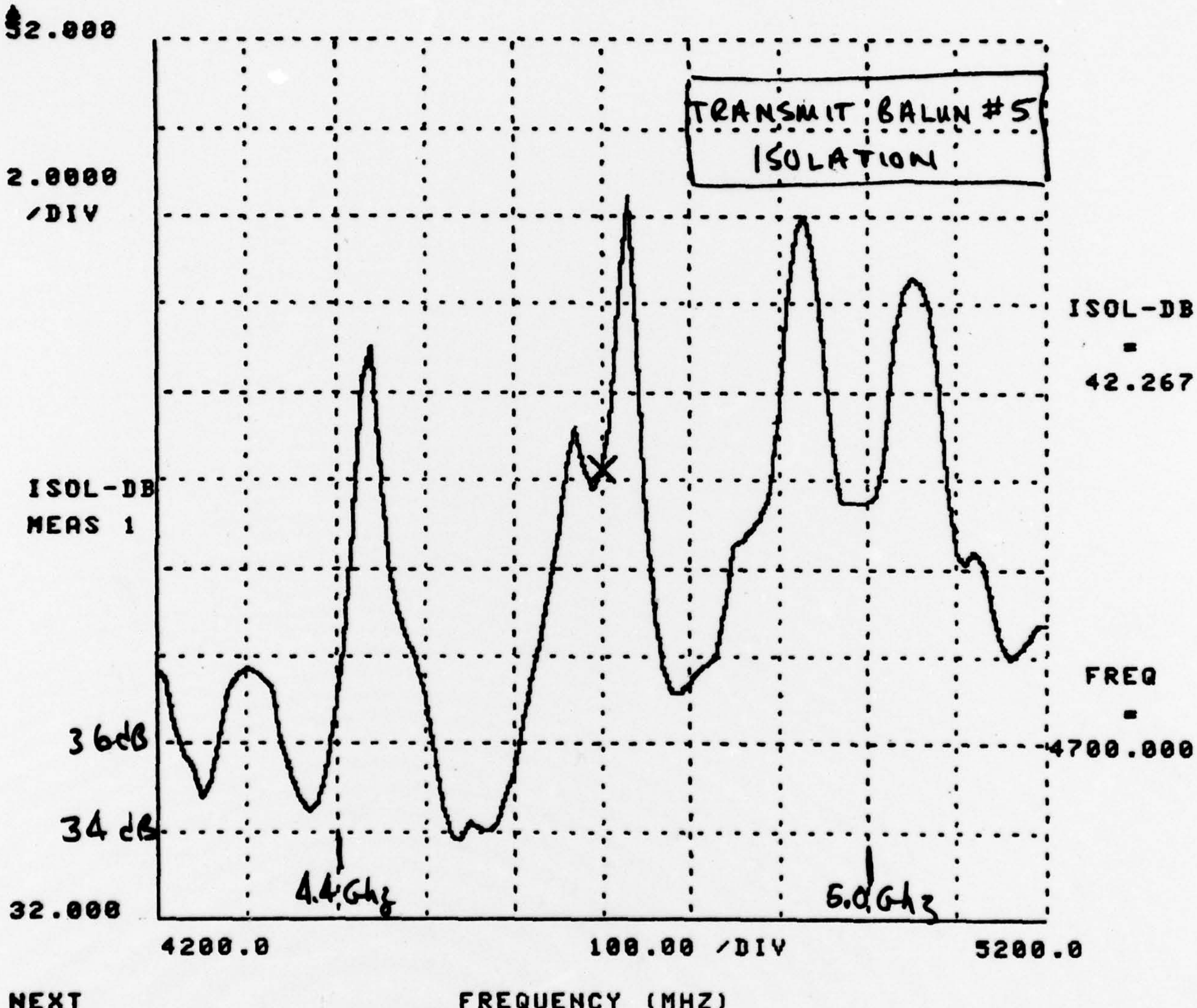


PHASED ARRAY
5-3-79
ANT. MEASUREMENT
WRAP AROUND/POLY SHEET
TRANS.#4/COMB. REC.
50.000
2.0000
/DIV
TRANSMIT BALUN #4
ISOLATION
ISOL-DB
=
44.718
ISOL-DB
MEAS 1
FREQ
=
4700.000
34 dB
32 dB
4.4Ghz
5.0Ghz
30.000
4200.0
100.00 /DIV
5200.0
NEXT
FREQUENCY (MHZ)

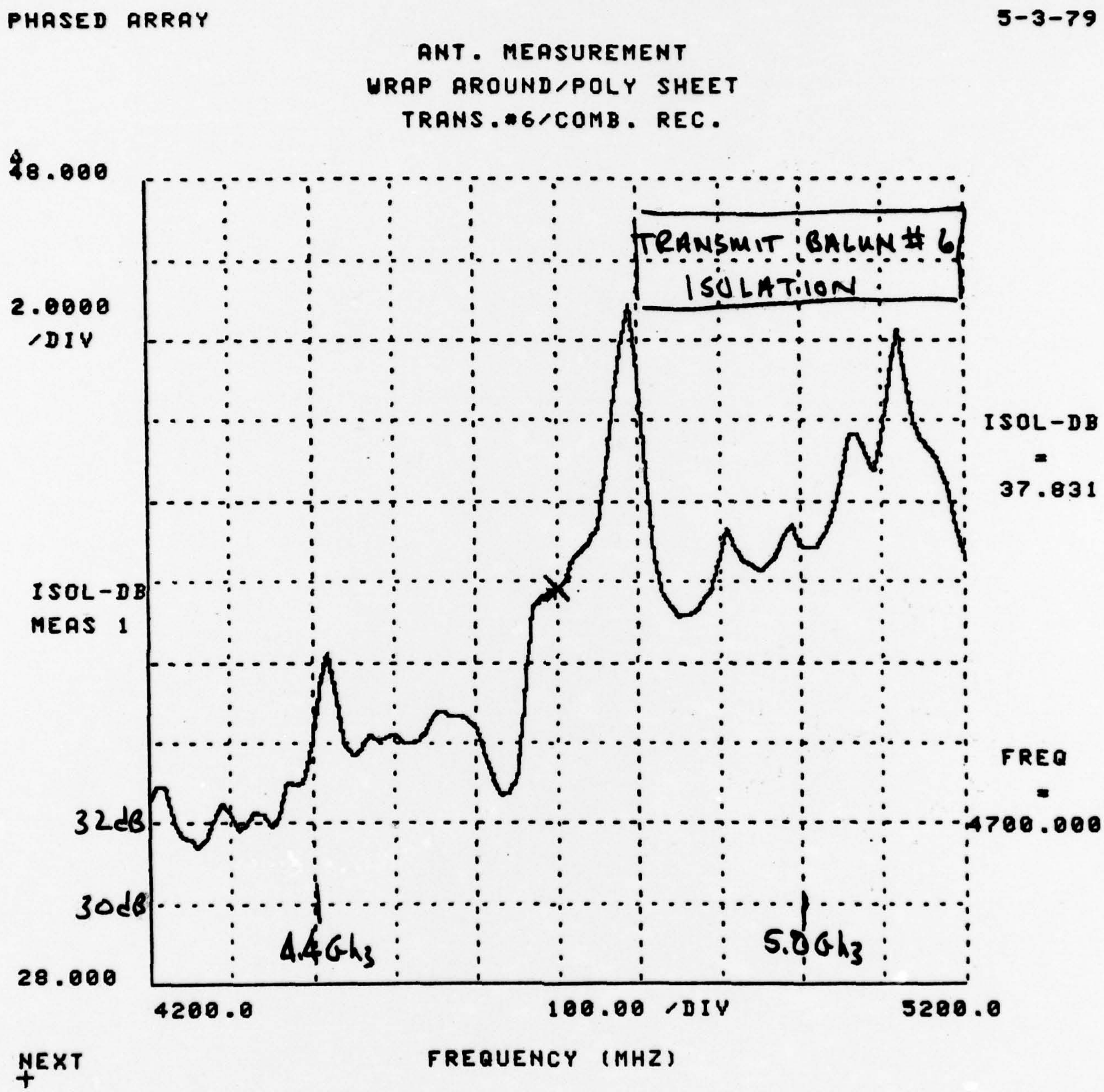
TP/8J

PHASED ARRAY 5-3-79

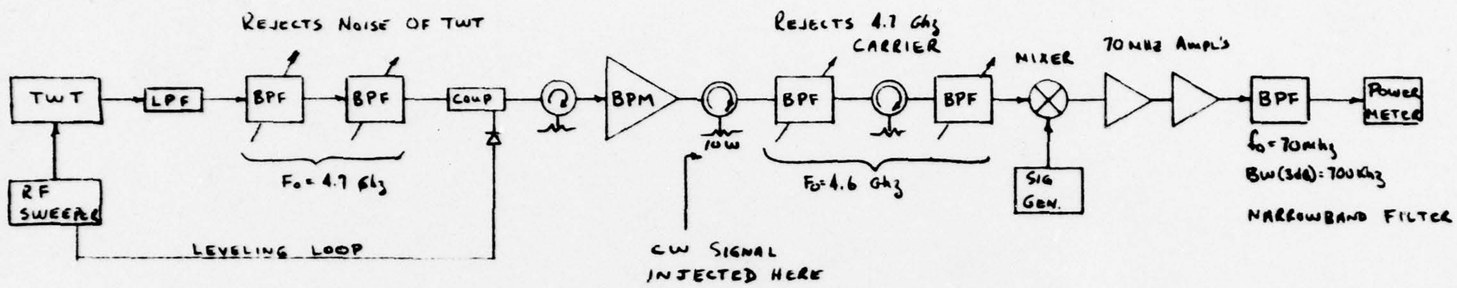
ANT. MEASUREMENT
WRAP AROUND/POLY SHEET
TRANS.#5/COMB. REC.



TP19h


PHASED ARRAY
5-3-79
ANT. MEASUREMENT
WRAP AROUND/POLY SHEET
TRANS.#6/COMB. REC.
48.000
2.0000
/DIV
ISOL-DB
MEAS 1
32dB
30dB
28.000
TRANSMIT BALUN #6
ISOLATION
4.4Ghz
5.0Ghz
ISOL-DB
=
37.831
FREQ
=
4700.000
4200.0
100.00 /DIV
5200.0
FREQUENCY (MHZ)
NEXT

TP 18L



TEST SET - BPM NOISE POWER OUTPUT

Fig 2

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TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION 2 PLACE	3 PLACE	ANGLES	DRAWN BY / DATE; CHECKED BY / DATE; APPROVED BY / DATE	ITT DEFENSE COMMUNICATIONS DIVISION	NUTLEY, NEW JERSEY	SIZE B	CODE IDENT. NO. 28528
							SCALE	REV. / SHEET TP19

D6215 B REV. 6/73

3.4.2.3 Antenna Polarization - (Set up - See Figure 4) Polarization of transmit and receive antenna signals shall be orthogonal, with transmit polarization at $+45^{o}$ and the receive polarization at -45^{o} (horizontal axis, 0^{o}; angles measured facing antenna).

Test Procedure - Polarization requirements will be demonstrated by comparison with the polarization of a known standard. A standard gain horn will be used for comparison. Although it is not specifically calibrated for polarization, its accuracy as a gain standard requires and implies accurate linear polarization properties. The polarization of the transmit and receive arrays will each be measured at 4.7 GHz.

Transmit Array	✓ Complies (V)
Receive Array	✓ Complies (V)

TP 20

3.4.2.4 Antenna Sidelobe Levels - (Set up - See Figure 4) The ratio of the antenna main lobe to any sidelobe shall be at least 15 dB.

Test Procedure: Sidelobes will be measured in the cardinal and intercardinal plane concurrently with the beamwidth. The test procedure is the same and is detailed in Section 3.4.2.1. Sidelobe data is read directly off the chart recording of power dB versus angle.

Sidelobe level of the transmit array complete with BPM's will also be conducted using the same procedure outlined in Section 3.4.2.1. Sidelobes will be measured as the difference in power between the peak in the main lobe and the peaks of the minor lobes as the array is rotated on the pedestal.

Active testing of the Receive Array is not required.

Sidelobe Performance with Amplifier Failures - For the transmit array, sidelobe pattern vs amplifier "failure" will be evaluated. This evaluation will be performed as follows.

Disconnect all amplifiers from the transmit baluns. Connect the 6 way power combiner to the transmit baluns. With the far field signal generator as the source, record the pattern of the transmit antenna in the cardinal plane and intercardinal plane at 4700 MHz.

Disconnect one (1) center balun (corresponding to amplifier A2) terminating it in 50 Ω loads and record the cardinal and intercardinal patterns.

Reconnect this balun, then disconnect one (1) edge balun (corresponding to amplifier A1). Terminate this balun in 50 Ω. Record the cardinal and intercardinal patterns.

All sidelobe testing will be conducted on a far-field, 1000 foot, outdoor range.

ANTENNA SIDELOBES[2]

I] PASSIVE TESTING / NO BPM's

	TX ARRAY			RX ARRAY		
FREQ	VERT[1]	HORIZ	INTER	VERT	HORIZ	INTER
4.40	15.0 dB	16.1 dB	19.1 dB	16.0 dB	16.3 dB	22.4 dB
4.55	15.6 dB	16.2 dB	21.1 dB	16.4 dB	15.7 dB	21.0 dB
4.70	14.9 dB	16.3 dB	20.0 dB	15.8 dB	14.1 dB	17.3 dB
4.85	15.2 dB	15.9 dB	20.0 dB	18.5 dB	14.1 dB	20.2 dB
5.00	14.9 dB	15.0 dB	20.2 dB	15.9 dB	15.4 dB	19.7 dB

1) VERTICAL = E PLANE , HORIZONTAL = H PLANE
2) HIGHEST SIDELOBE LEVEL, RELATIVE TO MAIN BEAM

II] SIDELOBE LEVEL FOR TX ARRAY WITH BPM's

	TX ARRAY		
FREQ	VERT	HORIZ	INTER
4.40	14.9 dB	15.0 dB	18.2 dB
4.55	15.3	15.2	20.0
4.70	14.5	16.8	19.5
4.85	15.5	15.5	19.0
5.00	14.8	17.0	18.5

III] SIDELOBE DEGRADATION AS A FUNCTION OF BPM FAILURE

A) INNER SUB-ARRAY BALUN DISCONNECTED

FREQ	VERT	HORIZ	INTER
4.70 Ghz	12. dB	11.1 dB	18 dB

B) OUTER SUB-ARRAY BALUN DISCONNECTED

FREQ	VERT	HORIZ	INTER
4.70 Ghz	14.3 dB	14.0 dB	18.0 dB

TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION 2 PLACE	3 PLACE	ANGLES	ANTENNA SIDELOBES
USED ON		CODE IDENT. NO. 28528	DWG. A SIZE	PHASED ARRAY
PREPARED BY	DATE			
CHECKED BY	DATE			SHEET TP21A

ITT DEFENSE COMMUNICATIONS DIVISION NUTLEY, NEW JERSEY

DRAWING NUMBER

D6215 A REV. 5/73

3.4.2.5 VSWR - The input VSWR of any element in the radiating matrix shall not exceed 1.5:1 over 4.4-5.0 GHz. The VSWR at the receive terminal shall not exceed 1.5:1 over 4.4-5.0 GHz.

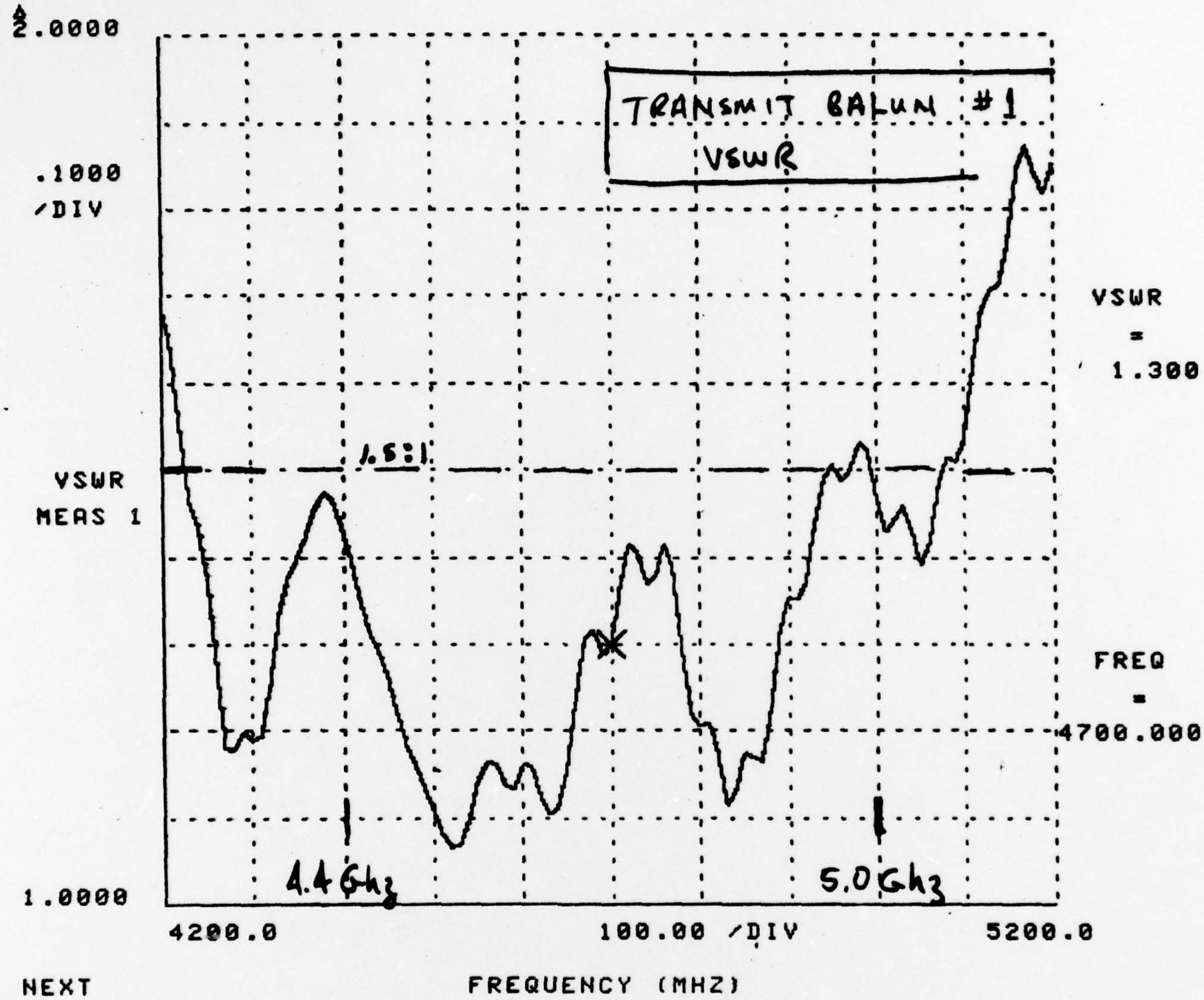
Test Procedure: VSWR will be tested on an indoor range using an Automatic Network Analyzer. A quasi-swept frequency range will be measured covering 4.4-5.0 GHz. The Receiver Array VSWR will be measured at its combiner output port. The transmit array will be measured without the BPM's and at each of the 6 Balun inputs.

Transmit Balun	1	1.53:1	Limit
	2	1.51:1	1.5:1.0
	3	1.98:1	
	4	1.71:1	
	5	1.89:1	
	6	2.31:1	
Receive Port		1.86:1	

TP22

PHASED ARRAY 5-3-79

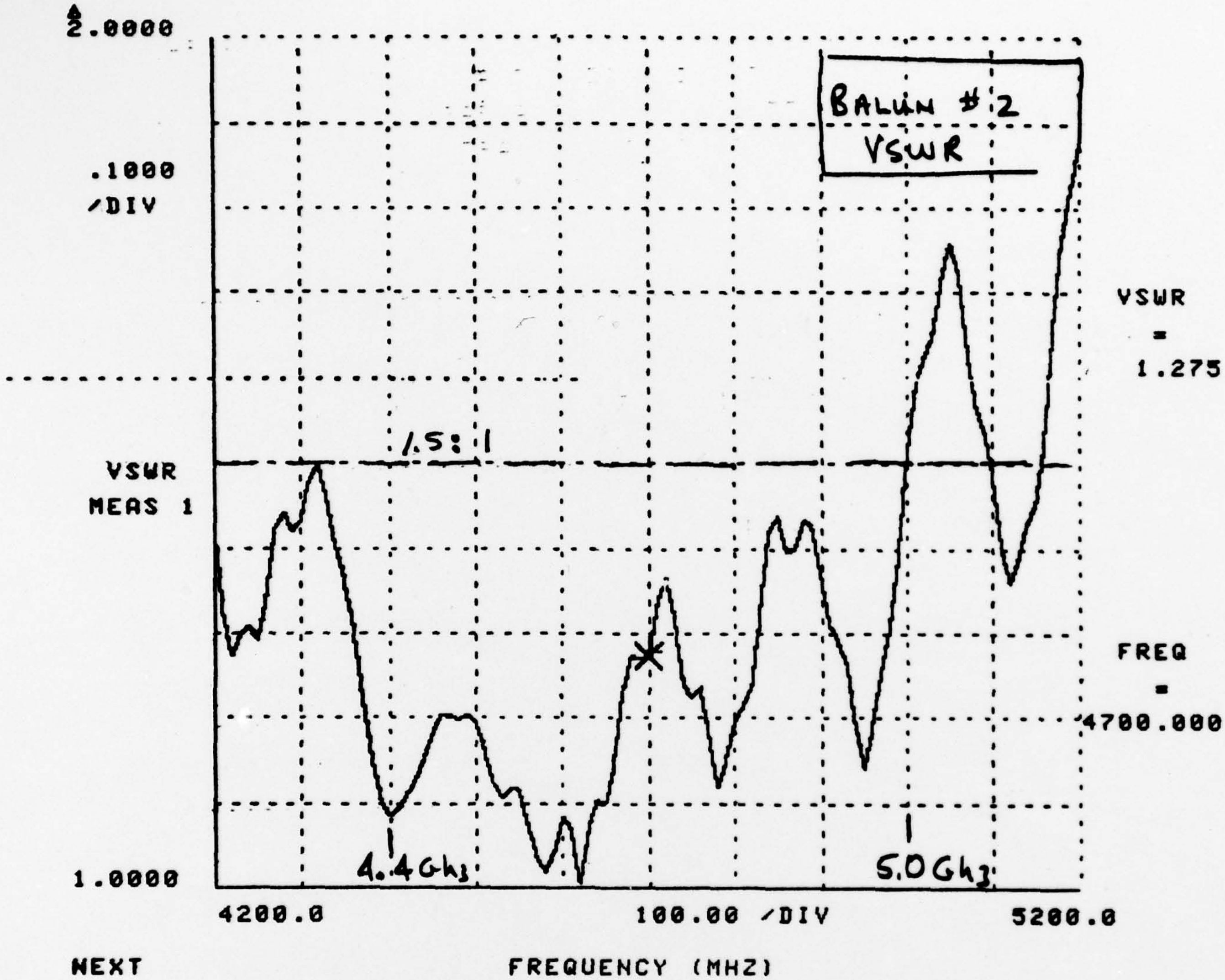
ANT. MEASUREMENT
WRAP AROUND/POLY SHEET
TRANS.#1/COMB. REC.



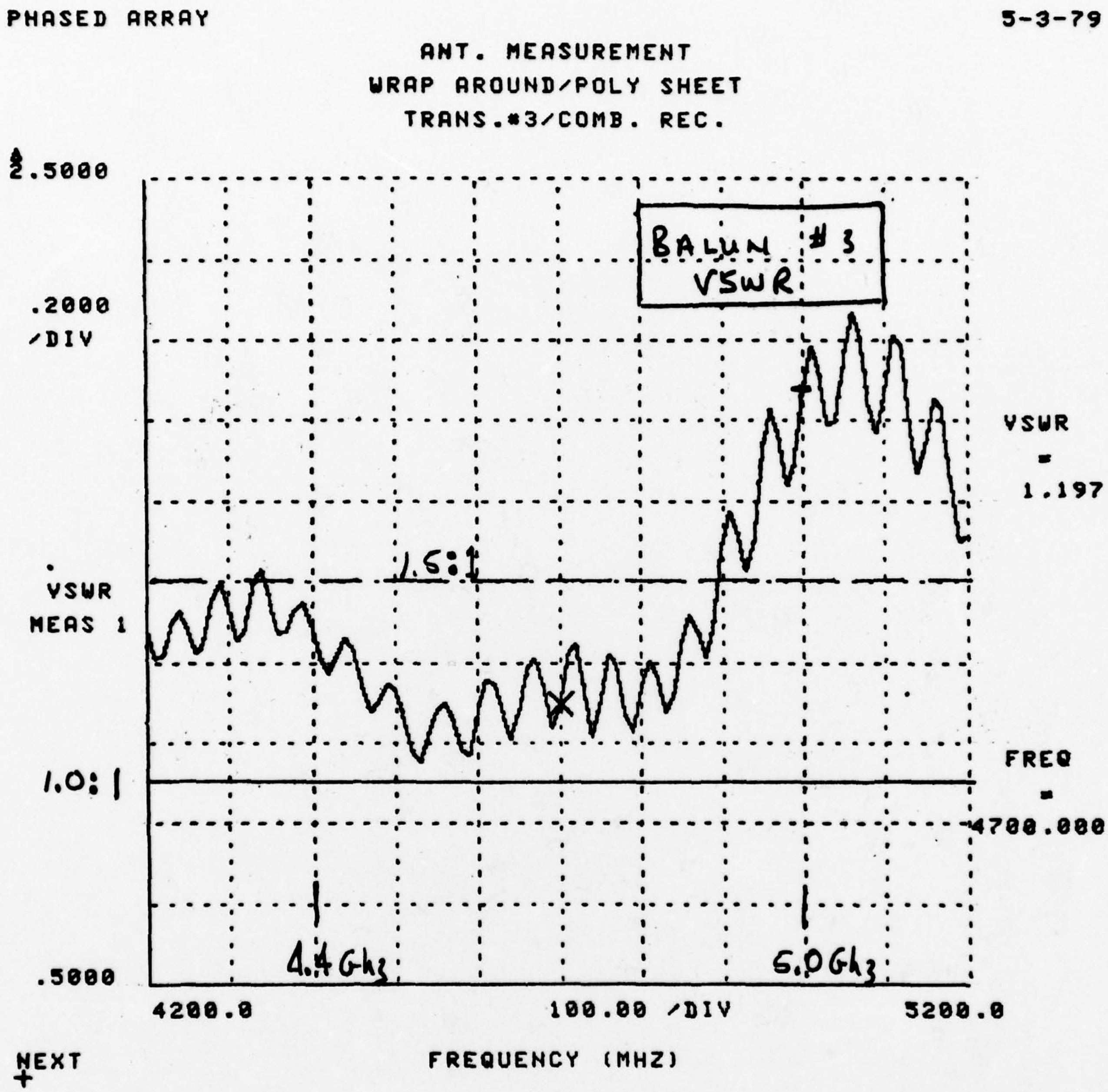
TP22A

PHASED ARRAY 5-3-79

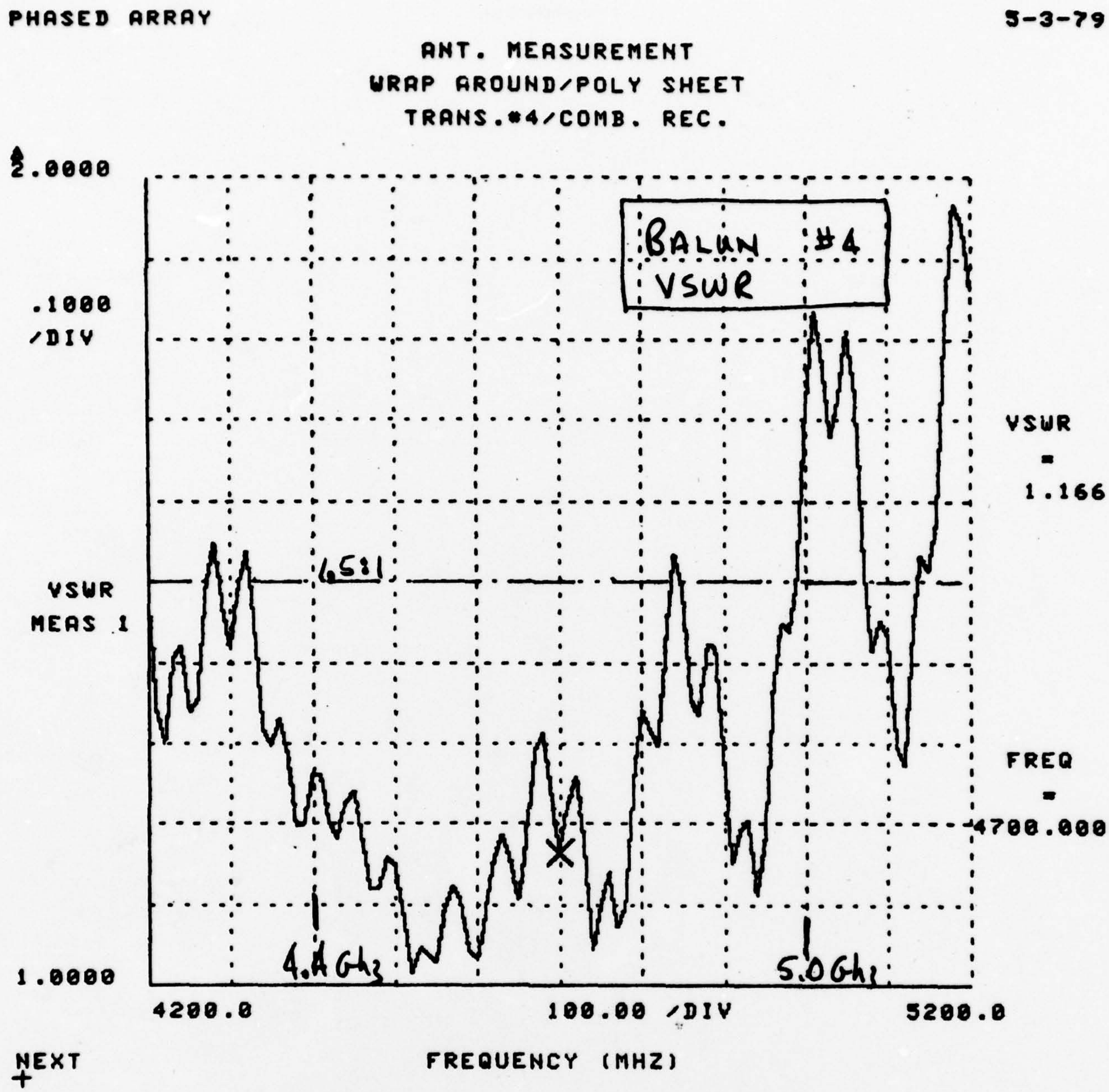
ANT. MEASUREMENT
WRAP AROUND/POLY SHEET
TRANS.#2/COMB. REC.



TP22B


PHASED ARRAY
5-3-79
ANT. MEASUREMENT
WRAP AROUND/POLY SHEET
TRANS.#3/COMB. REC.
2.5000
.2000
/DIV
VSWR
MEAS 1
1.0:1
.5000
BALUN #3
VSWR
1.5:1
4.4 Ghz
5.0 Ghz
VSWR
=
1.197
FREQ
=
4700.000
4200.0
100.00 /DIV
5200.0
NEXT
FREQUENCY (MHZ)

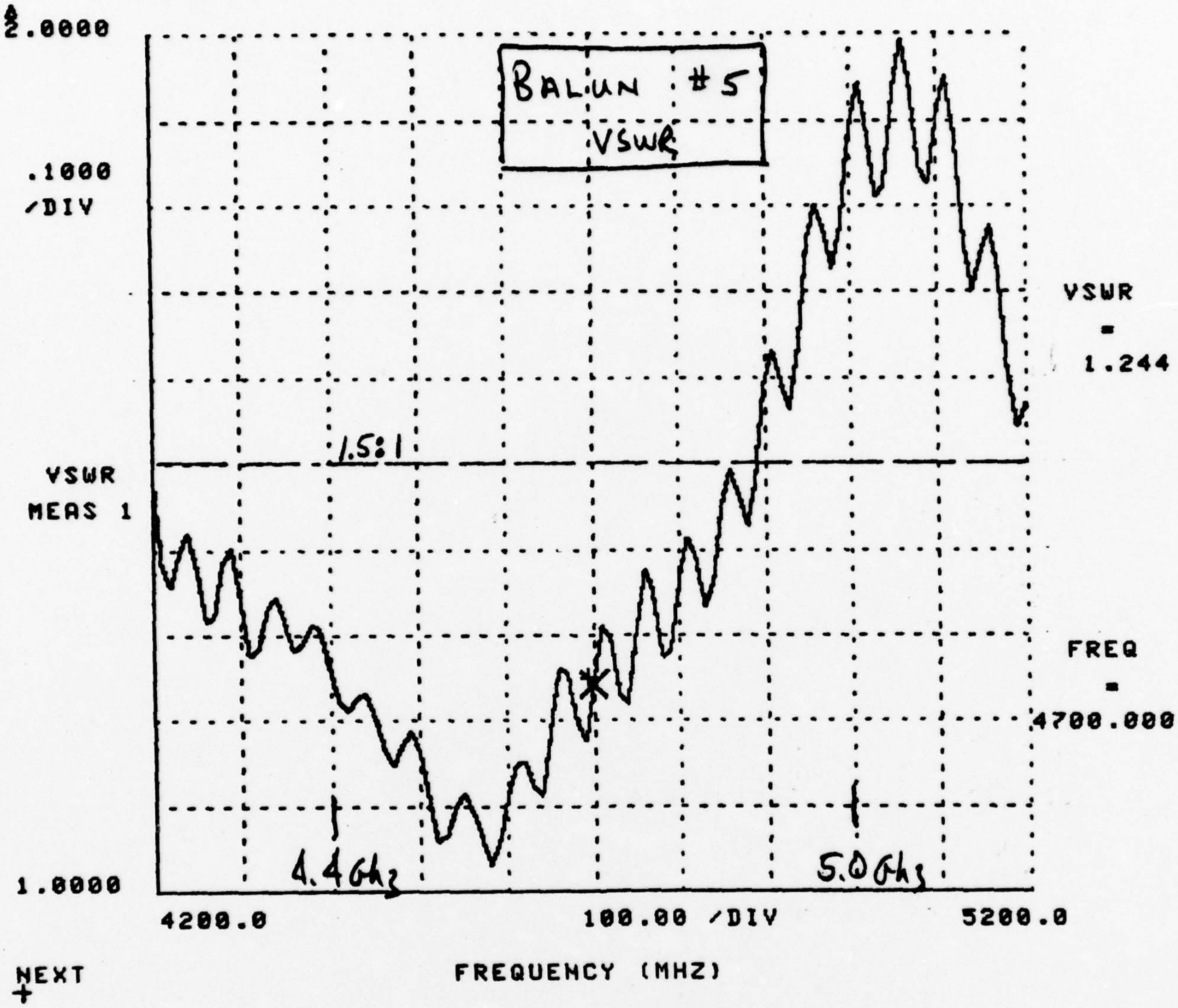
TA22C


PHASED ARRAY
5-3-79
ANT. MEASUREMENT
WRAP AROUND/POLY SHEET
TRANS.#4/COMB. REC.
2.0000
.1000
/DIV
VSWR
MEAS 1
1.0000
BALUN #4
VSWR
1.5:1
4.4 GHz
5.0 GHz
VSWR
=
1.166
FREQ
=
4700.000
4200.0
100.00 /DIV
5200.0
FREQUENCY (MHZ)
NEXT
+

TP22D

PHASED ARRAY 5-3-79

ANT. MEASUREMENT
WRAP AROUND/POLY SHEET
TRANS.#5/COMB. REC.

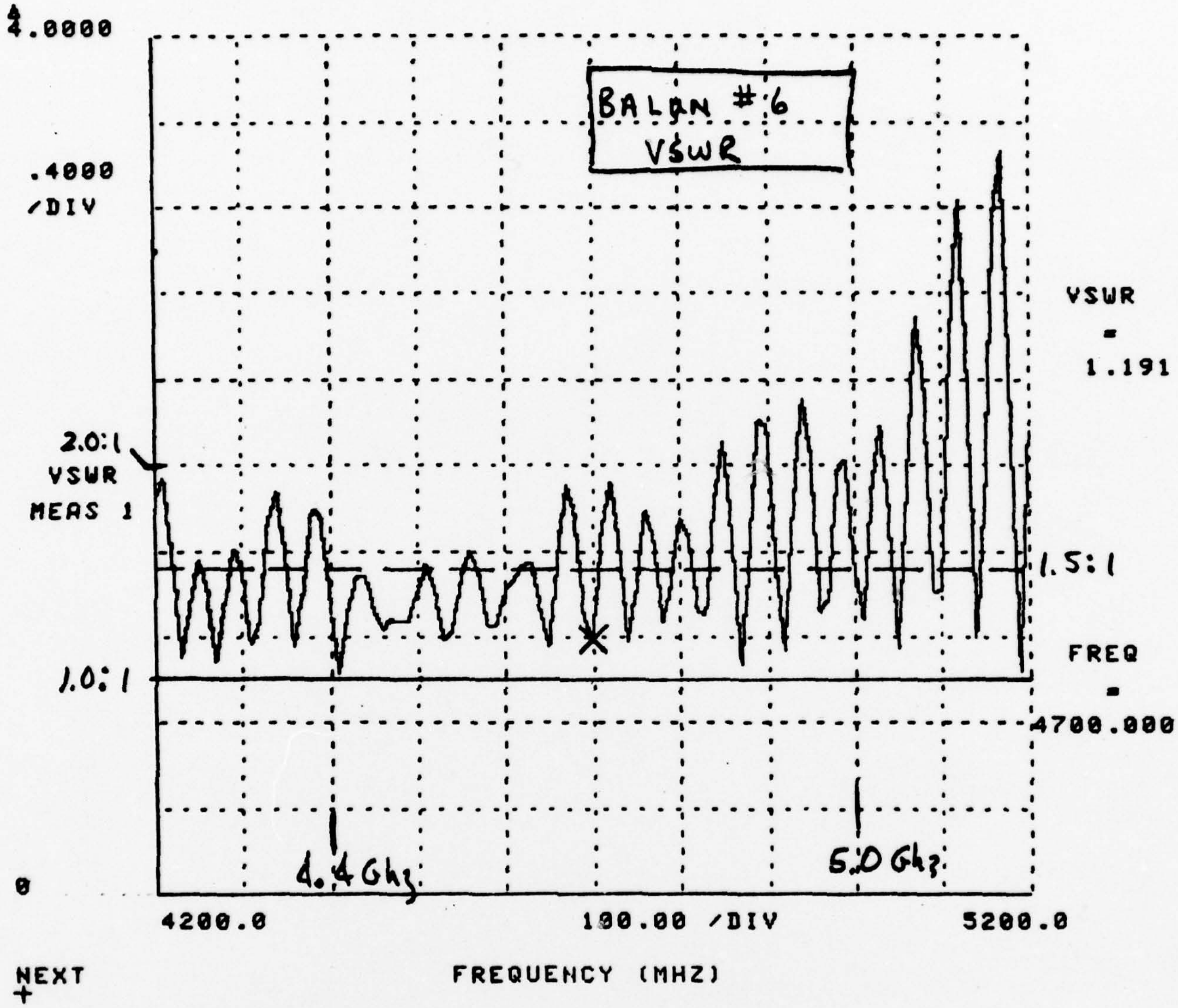


TA22E

PHASED ARRAY

5-3-79

ANT. MEASUREMENT
WRAP AROUND/POLY SHEET
TRANS.#6/COMB. REC.

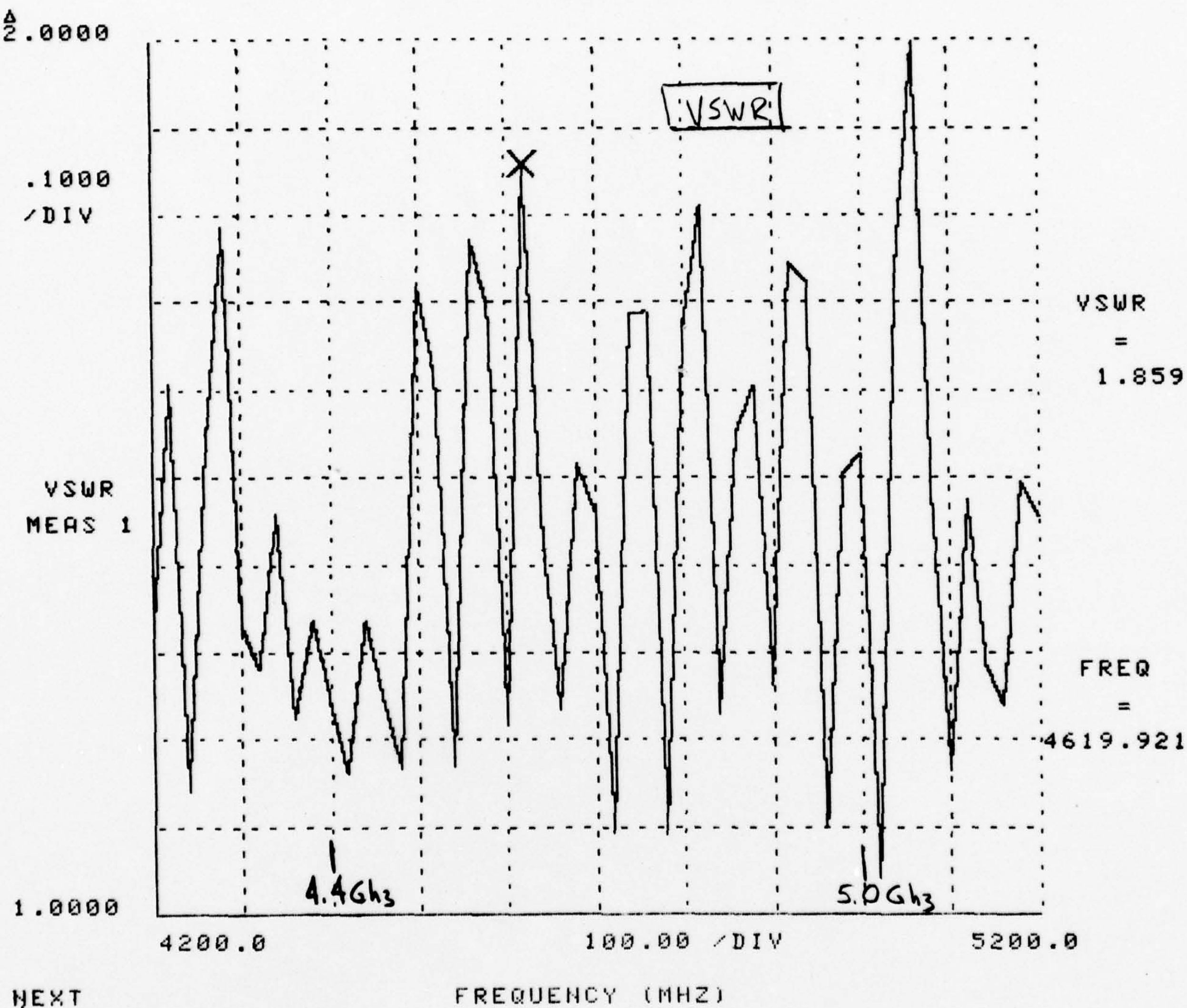


TP22F

PHASED ARRAY JUNE 12 1979

RECEIVE ARRAY

SER.01



TP22G

3.4.2.6 Amplifier Matrix Gain - The amplifier matrix of the Phased Array Antenna Amplifier shall meet the following spec's:

PIN	100 MW (nom)
POUT	10 Watts (min)
FREQ	4.4 - 5.0 GHz
EFF (DC-RF)	14% (min)
ERP	+70 dBm (min)

RF power into each of the six transmit antenna baluns will be measured and summed to determine total transmitter output power. Input power will be 100 MW over 4.4 - 5.0 GHz.

Freq	P_1	P_2	P_3	P_4	P_5	P_6	PTOT (Limit: 10W Min)
4.4 GHz	1.62 w	1.69 w	1.73 w	1.76 w	1.78 w	1.68 w	10.25 watt
4.7 GHz	1.59 w	1.69 w	1.62 w	1.75 w	1.62 w	1.68 w	9.95 watt
5.0 GHz	1.15 w	1.17	1.36 w	1.05 w	1.36 w	1.05 w	7.14 watt
4.9 Ghz	1.68 w	1.72 w	1.94 w	1.62 w	1.92 w	1.54 w	10.41 watt

At each frequency, total DC current will be measured to determine DC-RF efficiency,

$$N = \frac{\text{PTOT RF}}{V_{DC} \times I_{DC}} \times 100\%$$

Freq.	V_{DC}	I_{DC}	PTOT	N(%) (Limit: 14% Min)
4.4 GHz	8.5 v	6.86 a	10.25 w	17.6%
4.7 GHz	8.5 v	6.73 a	9.95 w	17.4%
5.0 GHz	8.5 v	6.26 a	7.14 w	13.4%
4.9 Ghz	8.5 v	6.14 a	10.41 w	18.2%

ERP

System ERP will be measured on the antenna range. The range will first be calibrated using a known power level and two standard gain antennas.

The procedure for system ERP measurement uses the same set-up, Figure 4, as for gain except the signal generator is connected to the standard gain horn at the turntable with a calibrated power meter, and a relative power meter is connected to the far field "source" antenna which now functions as a receiver. Steps are as follows:

AMPLIFIER MATRIX SUMMARY

TRANSMITTER CHAIN INCLUDING IPA

$P_{IN} = +20$ dBm[4]

	I_{TOT}[1]	P_{OUT}[2]	EFF[3]
4.4 Ghz	6.86 amp	10.25 w	17.6%
4.7 Ghz	6.73 amp	9.95 w	17.4%
4.9 Ghz	6.74 amp	10.41 w	18.2%
5.0 Ghz	6.26 amp	7.14 w	13.4%

$P_{IN} = +21$ dBm

	I_{TOT}	P_{OUT}	EFF
4.4 Ghz	6.93 a	10.75 w	18.2%
4.7 Ghz	6.82 a	10.19 w	18.4%
4.9 Ghz	6.74 a	10.11 w	18.5%
5.0 Ghz	6.31 a	7.24 w	14.1%

$P_{IN} = +22$ dBm

	I_{TOT}	P_{OUT}	EFF
4.4 Ghz	6.94 a	10.93 w	18.5%
4.7 Ghz	6.92 a	11.02 w	18.7%
4.9 Ghz	6.74 a	10.73 w	18.7%
5.0 Ghz	6.33 a	7.81 w	14.5%

$P_{IN} = +23$ dBm

	I_{TOT}	P_{OUT}	EFF
4.4 Ghz	7.04 a	11.01 w	18.4%
4.7 Ghz	6.94 a	11.18 w	19.0%
4.9 Ghz	6.74 a	10.77 w	18.8%
5.0 Ghz	6.37 a	8.02 w	14.8%

1) TOTAL DC CURRENT @ 8.5 v
2) Sum OF RF power at 6 Tx Baluns
3) DC-RF Eff

$$\eta = \frac{P_{OUT}}{I_{TOT} \times 8.5} \times 100$$

4) FROM AN/GRC-143 TRANSMITTER

J.I. 5/12/79

TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION 2 PLACE	DECIMAL DIMENSION 3 PLACE	ANGLES	AMPLIFIER MATRIX

USED ON	CODE IDENT. NO.	DWG. SIZE	
PREPARED BY / DATE	28528	A	PHASED ARRAY
CHECKED BY / DATE			SHEET TP23A

DRAWING NUM

NUTLEY, NEW JERSEY

DEFENSE COMMUNICATIONS DIVISION

ITT

D5215 A REV. 5/73

1. Apply a known power (P_c) to the SGH, peak the received power by adjusting turntable and record the received power (P_s) as reference.

2. Connect array under test (UUT) and adjust for full transmitted power (Pt) as previously recorded. Adjust turntable for peak received power and record the received power (Pa) as a decibel difference from reference power (Ps).

3. Calculate ERP as:

$$ERP_{Array} = ERP_{SGH} \times \frac{Pa}{Ps} = G_{SGH} P_c \frac{Pa}{Ps}$$

or

$$ERP_A(dBM) = G_{SGH}(dB) + P_c(dBM) + Pa\ (dB) - Ps\ (dB)$$

<u>ERP Vs. Amplifier Failure</u>

Evaluation of ERP due to amplifier failure is a prime consideration for this system. ERP will be measured per above procedure. Baluns will be disconnected from amplifier output one at a time. The unused BPM output and balun will be terminated in 50 Ω.

Procedure:

Set system for operation @ 4700 MHz and measure ERP per above procedure.

1) Disconnect the RF input to one balun corresponding to amplifier A1 output. Terminate this balun in 50 Ω. Terminate the unused BPM splitter output in 50 Ω. Record reduction in meter reading.

2) Reconnect all baluns. Disconnect the RF input to one balun corresponding to amplifier A2 output. Terminate the balun and unused output of BPM splitter in 50 Ω. Record reduction in meter reading.

The difference between ERP with all amplifier connected and the respective meter reading reduction with amplifier disconnected is the ERP for those conditions.

Repeat the above procedure at 4400 & 5000 MHz.

*In calculating total transmitted power at the balun inputs, phase differences are not considered. The coax cable lengths from the amplifiers to the transmit baluns were designed to compensate for the difference in the feed line lengths within the transmit

TP 24

ERP MEASUREMENTS

I] All BPM's OPERATING

$$ERP = P_c + P_A - P_S + G_{SGH}$$

where: P_c = Power Input to Standard Gain Horn

P_A = Rec'd power from PHASED ARRAY

P_S = Rec'd power from Standard Gain Horn

G_{SGH} = Gain of Standard Gain Horn

FREQ	P_c (dBm)	P_A (dBm)	P_S (dBm)	G_{SGH} (dB)	ERP (dBm)
4.40 Ghz	+40.18 dBm	-13.3 dBm	-25.6 dBm	17.9 dB	70.4 dBm
4.45	40.54	-12.9	-25.6	17.95	71.2 dBm
4.50	40.66	-12.8	-26.0	18.00	71.9 dBm
4.55	40.27	-13.2	-26.8	18.05	71.9 dBm
4.60	40.25	-13.8	-27.3	18.10	71.9 dBm
4.65	40.45	-14.2	-26.4	18.18	70.8 dBm
4.70	40.48	-14.2	-25.8	18.25	70.3 dBm
4.75	40.45	-13.6	-26.0	18.32	71.2 dBm
4.80	40.40	-13.0	-25.9	18.40	71.7 dBm
4.85	40.67	-13.0	-25.2	18.45	71.3 dBm
4.90	40.66	-13.4	-25.9	18.50	71.7 dBm
4.95	39.94	-14.0	-25.8	18.58	70.3 dBm
5.00	40.23	-15.0	-25.6	18.65	69.5 dBm

TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION 2 PLACE	DECIMAL DIMENSION 3 PLACE	ANGLES	ERP
USED ON	CODE IDENT. NO. 28528	DWG. SIZE A	PHASED ARRAY	
PREPARED BY / DATE				
CHECKED BY / DATE			SHEET TP24A	

array. Thus, the relative phase (cable length) from amplifiers to baluns differs depending upon balun location. Thus, phase considerations in calculating total power at the balun inputs is not valid. The phase considerations are included in the effective radiated power measurements.

ERP MEASURMENTS

II] ERP LOSS VS BPM FAILURE

A) INNER SUB-ARRAY BALUN DISCONNECTED

FREQ	LOSS IN ERP
4.4 Ghz	1.5 dB
4.7 Ghz	1.6 dB
5.0 Ghz	1.8 dB

B) OUTER SUB-ARRAY BALUN DISCONNECTED

FREQ	LOSS IN ERP
4.4 Ghz	1.5 dB
4.7 Ghz	1.8 dB
5.0 Ghz	1.0 dB

SEE PARA 3.4.2.4 FOR SIDELOBE DEGRADATION

TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION 2 PLACE	3 PLACE	ANGLES	ERP
USED ON	CODE IDENT. NO. 28528	DWG. A SIZE	PHASED ARRAY	
PREPARED BY DATE				
CHECKED BY DATE			SHEET TP24C	

----ERP ANALYSIS---
SCALE MODEL

TOTAL NUMBER OF FAILURES=0

FAILURES A	FAILURES B	ΔP (dB)	ΔG (dB)	ΔERP (dB)
.0	.0	-.00	.00	-.00

AVG LOSS IN ERP(dB)=-.01

TOTAL NUMBER OF FAILURES=1

FAILURES A	FAILURES B	ΔP (dB)	ΔG (dB)	ΔERP (dB)
.0	1.0	-.79	-1.15	-1.94
1.0	.0	-.79	-.12	-.92

AVG LOSS IN ERP(dB)=-1.43

TOTAL NUMBER OF FAILURES=2

FAILURES A	FAILURES B	ΔP (dB)	ΔG (dB)	ΔERP (dB)
.0	2.0	-1.76	-2.68	-4.44
1.0	1.0	-1.76	-1.34	-3.10
2.0	.0	-1.76	-.18	-1.94

AVG LOSS IN ERP(dB)=-3.16

TOTAL NUMBER OF FAILURES=3

FAILURES A	FAILURES B	ΔP (dB)	ΔG (dB)	ΔERP (dB)
.0	3.0	-3.01	-4.95	-7.96
1.0	2.0	-3.01	-3.01	-6.02
2.0	1.0	-3.01	-1.43	-4.44

AVG LOSS IN ERP(dB)=-6.14

TOTAL NUMBER OF FAILURES=4

FAILURES A	FAILURES B	ΔP (dB)	ΔG (dB)	ΔERP (dB)
.0	4.0	-4.77	-9.21	-13.98
1.0	3.0	-4.77	-5.69	-10.46
2.0	2.0	-4.77	-3.19	-7.96

AVG LOSS IN ERP(dB)=-10.8

TOTAL NUMBER OF FAILURES=5

FAILURES A	FAILURES B	ΔP (dB)	ΔG (dB)	ΔERP (dB)
1.0	4.0	-7.78	-12.22	-20.00
2.0	3.0	-7.78	-6.20	-13.98

AVG LOSS IN ERP(dB)=-16.99

3.4.2.7 Amplifier Matrix Input VSWR - VSWR measured into system input port shall not exceed 1.5:1 over 4.4 - 5.0 GHz.

VSWR will be determined by measuring the level of the reflected power using a directional coupler. A VSWR of 1.5:1 corresponds to a return loss of at least 14 dB.

1.36:1 1.5:1.0 (14 dB min)

3.4.2.8 Spurious Radiation (Harmonics) - Spurious radiation from amplifier matrix shall be at least 80 dB below carrier.

A This parameter is measured at the BPM level with its' low pass filter installed. If the LPF is unavailable, this parameter will be measured and adjusted by the LPF rejection.

		Spurious Radiation		
Frequency	4.4 GHz	-88	dbc	[with 50 dB LPF Rejection at 8.8 Ghz]
	4.7 GHz	-95	dbc	[with 55 dB LPF Rejection at 9.4 Ghz]
	5.0 GHz	-100	dbc	Limit: 80 dBc [with 60 dB LPF Rejection at 10 Ghz]

Spurious radiation out of each BPM will be measured on a spectrum analyzer.

— Refer to Appendix A for detailed measurements —

3.4.2.9 Parasitic Oscillation - No parasitic oscillations shall exist within any RF amplifier module.

The existence of parasitic oscillations will be checked for the IPA and each of the BPM's using a spectrum analyzer. This test will be conducted for various drive levels. This test will be conducted before the amplifiers are integrated into the system. With the amplifiers set up per Figure 1, the spectrum analyzer will display the slow swept response over the 4.4 - 5.0 GHz band. As RF input level is varied, the response will be observed for oscillation.

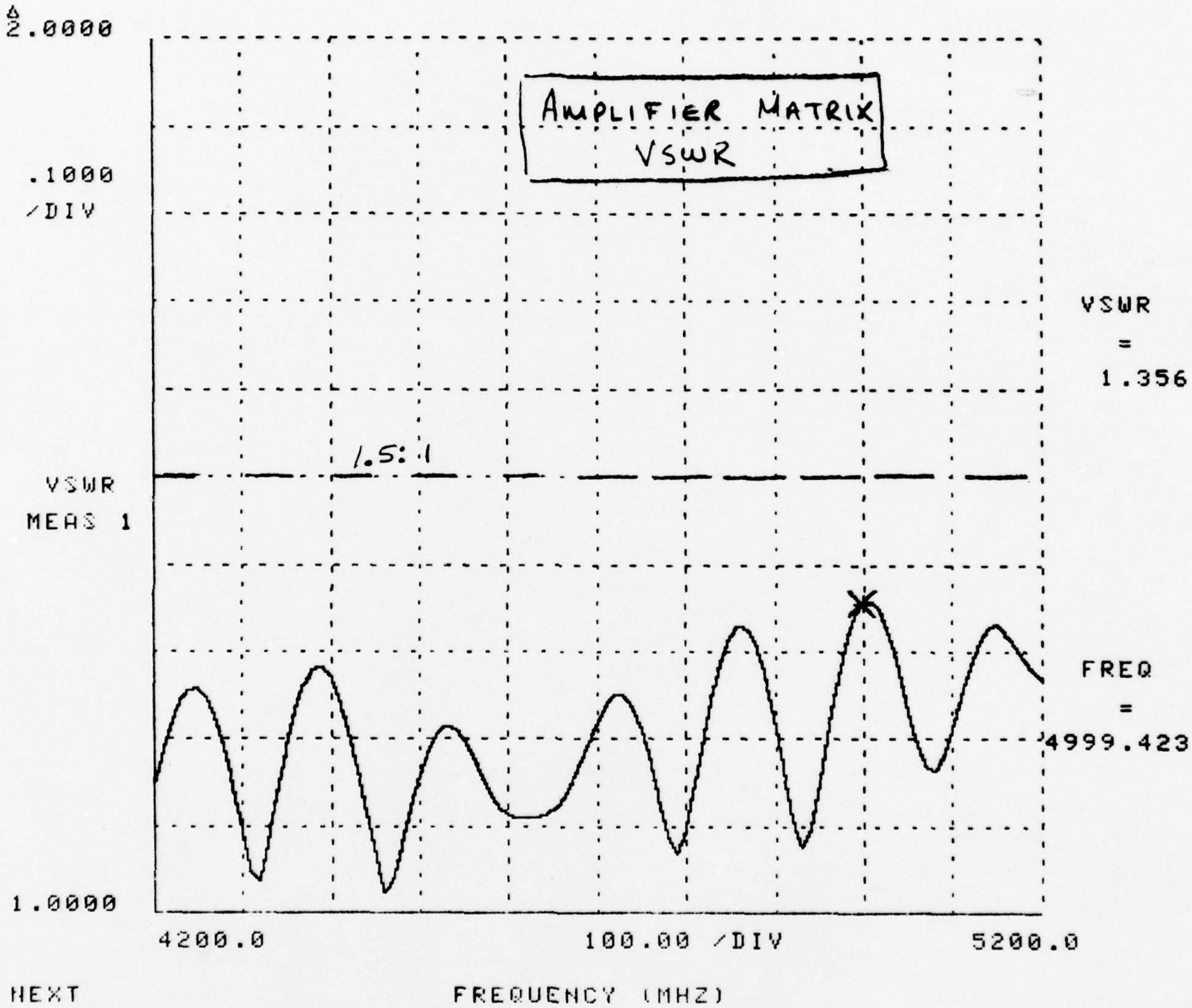
IPA No Oscillations	✓	Complies (V)
BPM A1	✓	Complies (V)
BPM A2	✓	Complies (V)
BPM A3	✓	Complies (V)

TP25

PHASED ARRAY 5-10-79

CONTROL CABINET J-4

RF INPUT



TP25A

3.4.2.10 Antenna-Amplifier MTBF - Design objective for the MTBF shall be 4000 hrs. A 3 dB loss in ERP shall be considered a failure.

The system MTBF has been computed and was presented in the Preliminary Design Plan. Section 2.7.3.1 This calculation indicates an MTBF of 3473 hr.

As part of the Final Report (CDRL-A003) on MTBF estimate for a 1 KW system will be provided. This evaluation will include such techniques as redundancy in order to attain a 4000 hour MTBF.

3.4.2.11 Amplifier Bandwidth - RF amplifier matrix shall have broadband non-tunable modules covering 4.4 - 5.0 GHz. All antenna amplifier modules shall be interchangeable.

Each amplifier in the amplifier matrix has been designed for, and will be tested over, the full 4.4 - 5.0 GHz band. Full bandwidth coverage will be obtained without remote tuning.

Each of the three antenna mounted BPM's are interchangeable both physically and electrically. System design is based upon equal power output from each of the antenna amplifiers. Aperture tapering is obtained with power distribution on the antenna. Full band performance is demonstrated by swept measurement at each

A BPM. See Appendix A for Detailed Amplifier Test Data.

	4.4 - 5.0 GHz Bandwidth	
BPM A1	✓	Complies (V)
BPM A2	✓	
BPM A3	✓	

TP27

3.4.2.12 System Degradation Alarm - A control panel shall be furnished which will permit the control and status display of all necessary electrical functions.

A control panel will be included as part of the control cabinet. It will include a micro-ammeter which will provide a positive up-scale reading to indicate acceptable performance. A multi-position switch will select which function is displayed on the meter. The functions are: Power Supply Output Voltage (pos & neg)

IPA Output Power

BPM Output Power (3).

Control Panel ✓ Complies (V)

TP28

3.4.3 Power - Supply voltage shall be internally regulated and operated from 120/230 volt ±10% (RMS) 50-60 Hz single phase. Total input power to the system shall not exceed 1 KW.

Supply voltage required for the Phase Array Antenna Amplifier is 120/230 volt ±10% (RMS), 50-60 Hz single phase. Two internal power supplies provide the required +9 VDC and -9 VDC for the system.

Total AC power input to the system will be measured using a Weston 432 wattmeter.

155 Watts

Limit 1000 watts

6.5% AC-RF EFFICIENCY
SEE PARA. 3.4.2.6 P_{TOTAL}

DC-RF Efficiency = 18% (typical) [see para 3.4.2.6]

TP29

DCD ... (N) ... 1/68

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DRAWING NUMBER

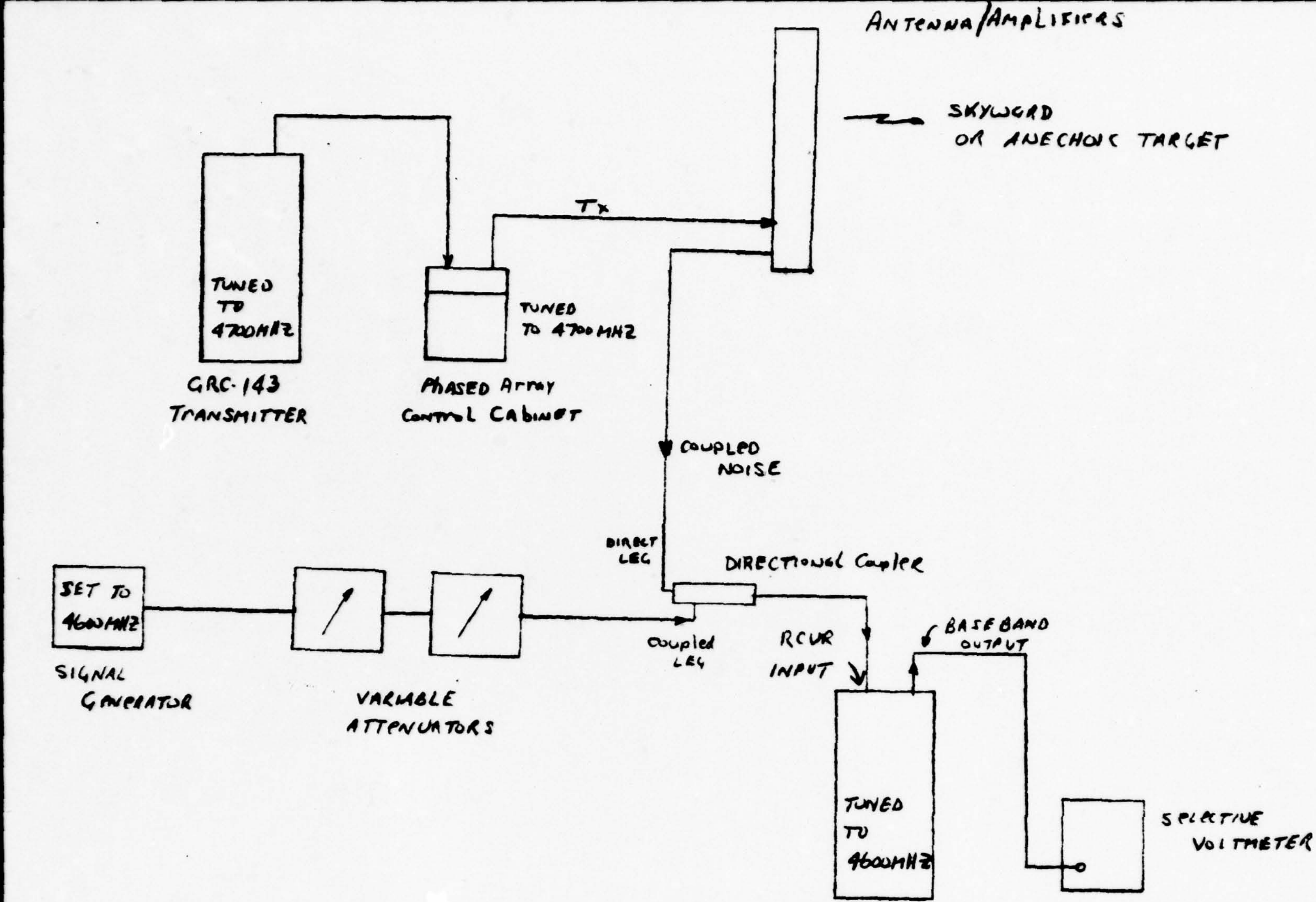


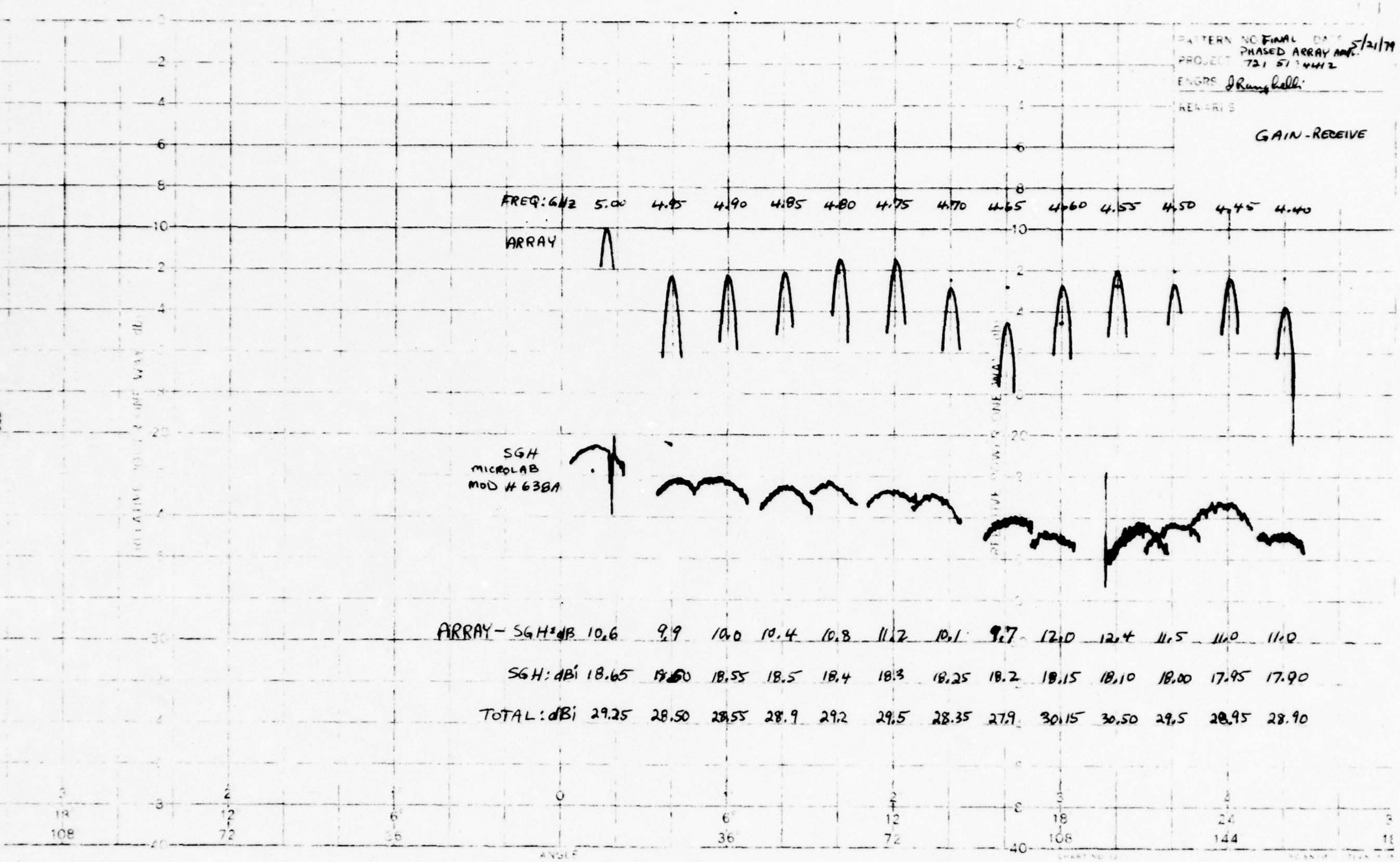
FIGURE 5 NOISE QUIETING

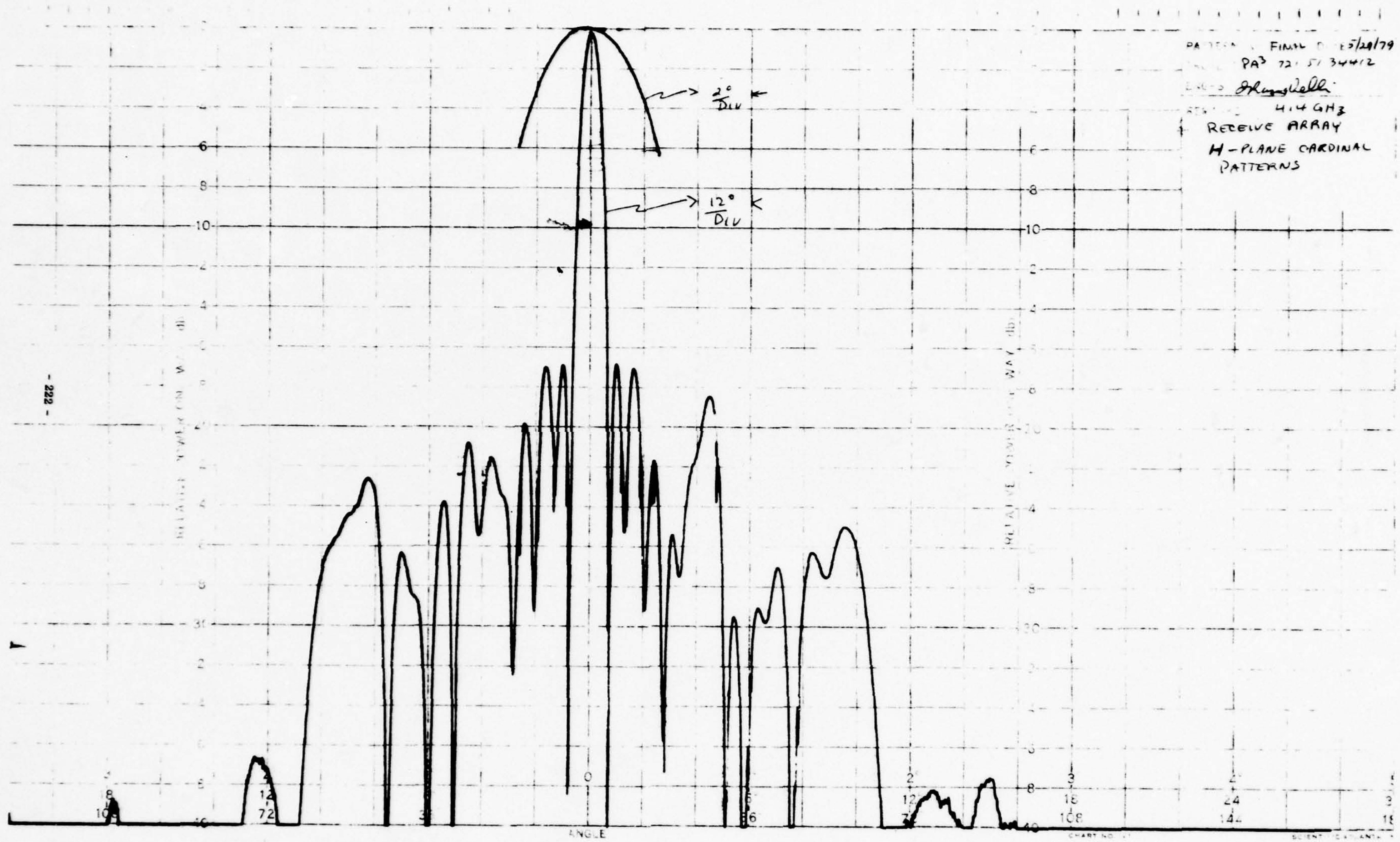
PREPARED BY	SIZE	CODE IDENT NO.	DWG. NO.
CHECKED BY	A	28528	
		REV.	SHEET TP30

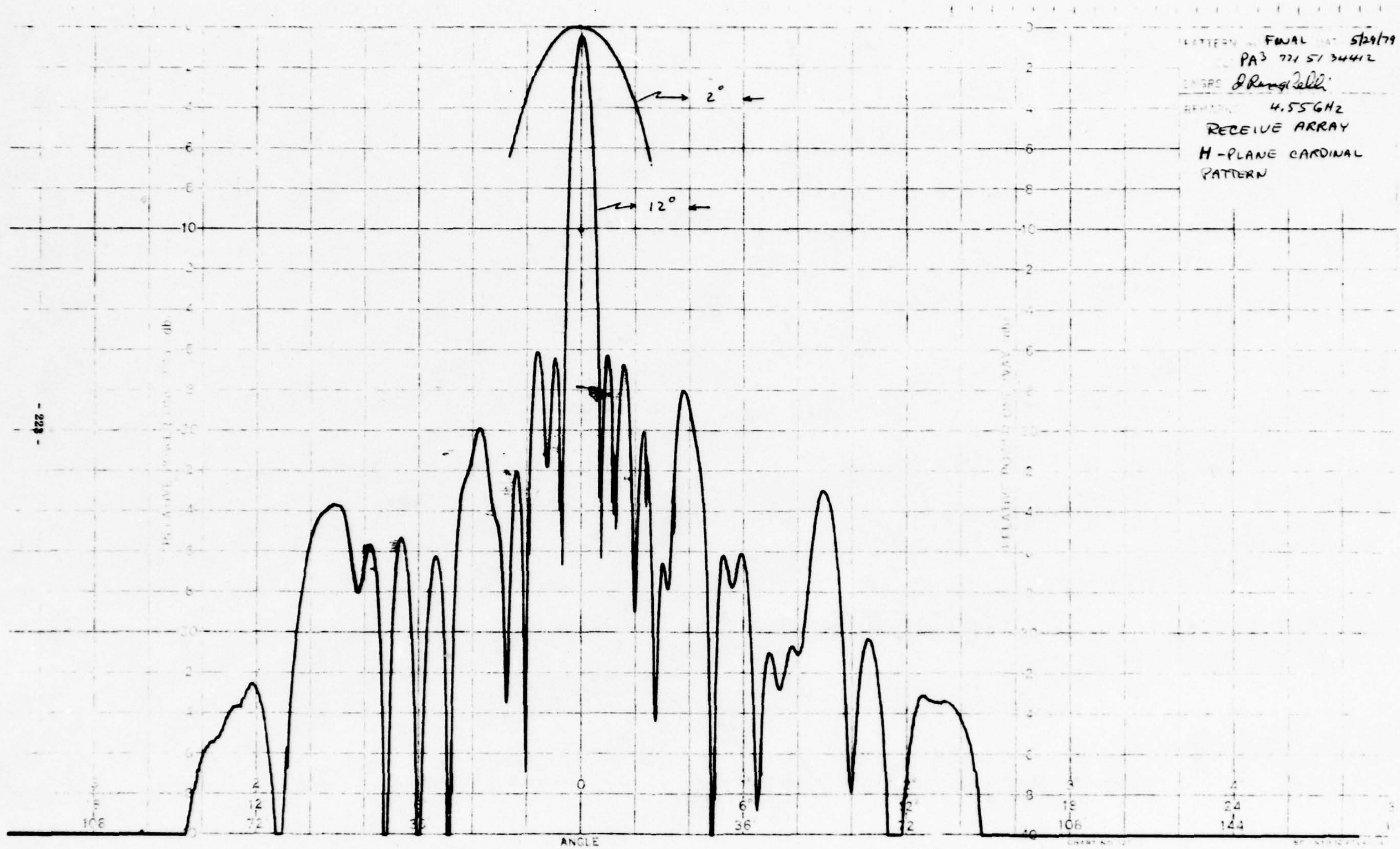
ANTENNA GAIN AND SIDELOBE PATTERNS
RECEIVE ARRAY

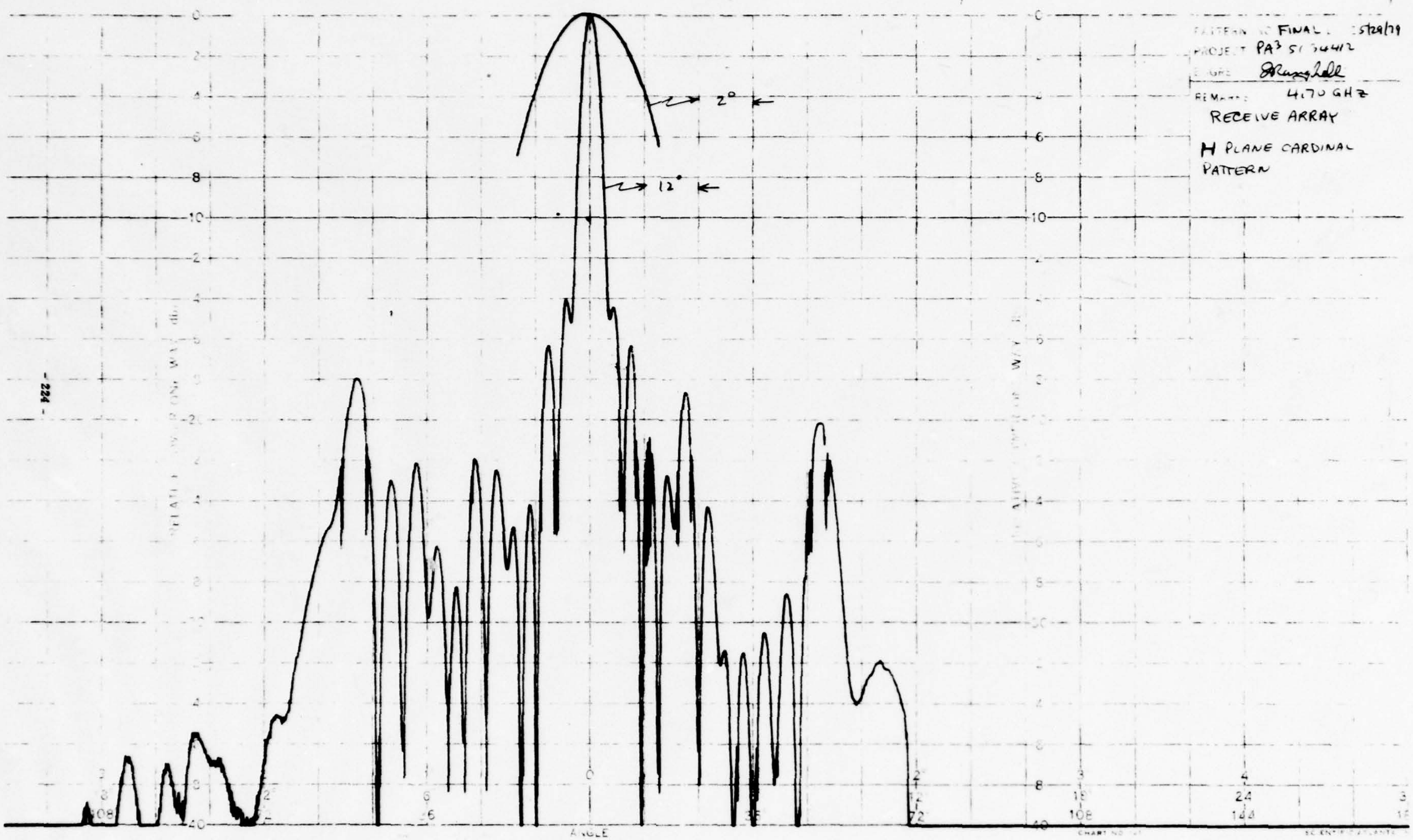
- Assembled in Final Configuration less the G10 Epoxy Fiber Glass Radome

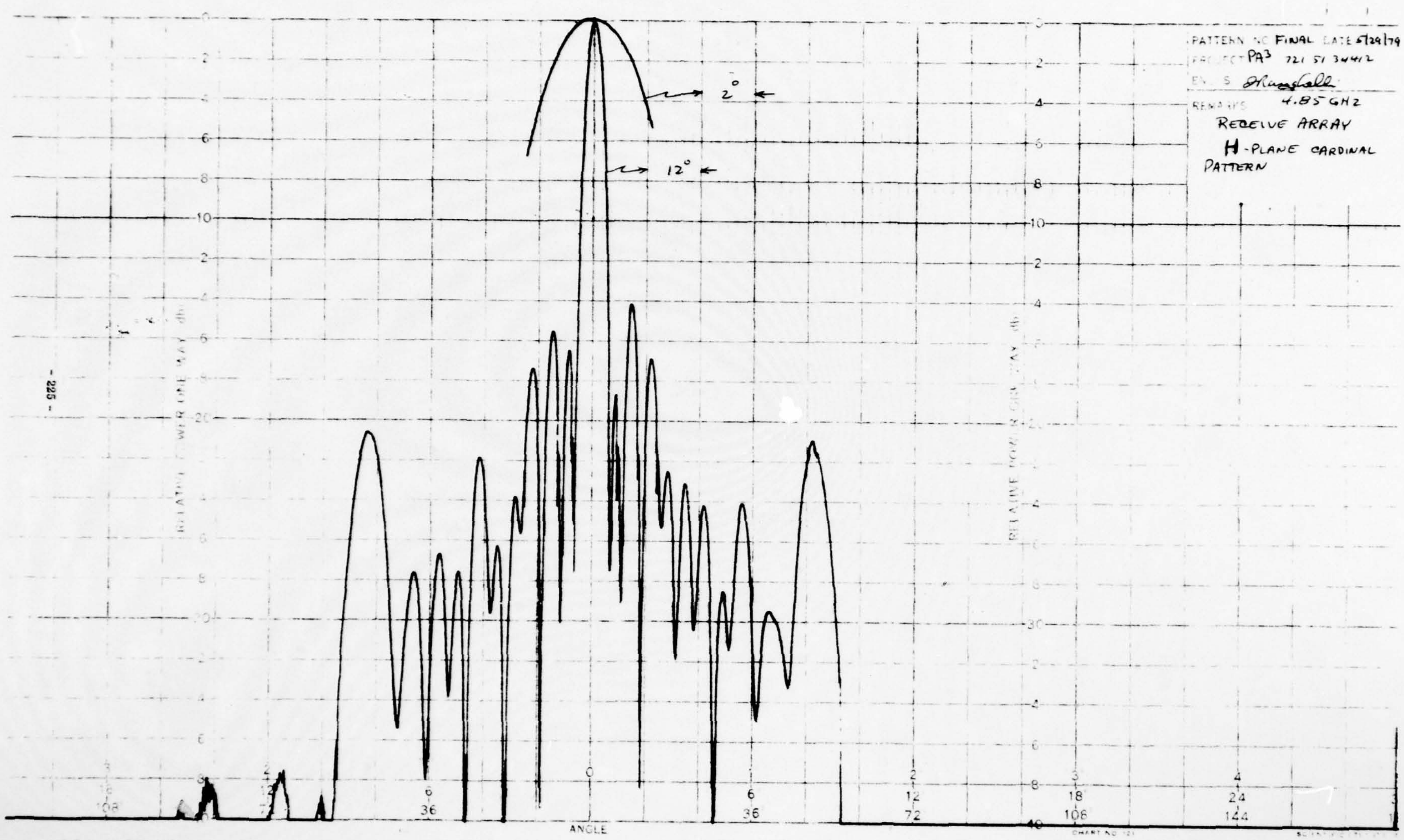
Gain	13 Frequencies
Sidelobes	
H Plane	1 Frequency/Pattern
E Plane	5 Patterns each plane
Intercardinial Plane	(4.4, 4.55, 4.7, 4.85, 5.0 GHz)

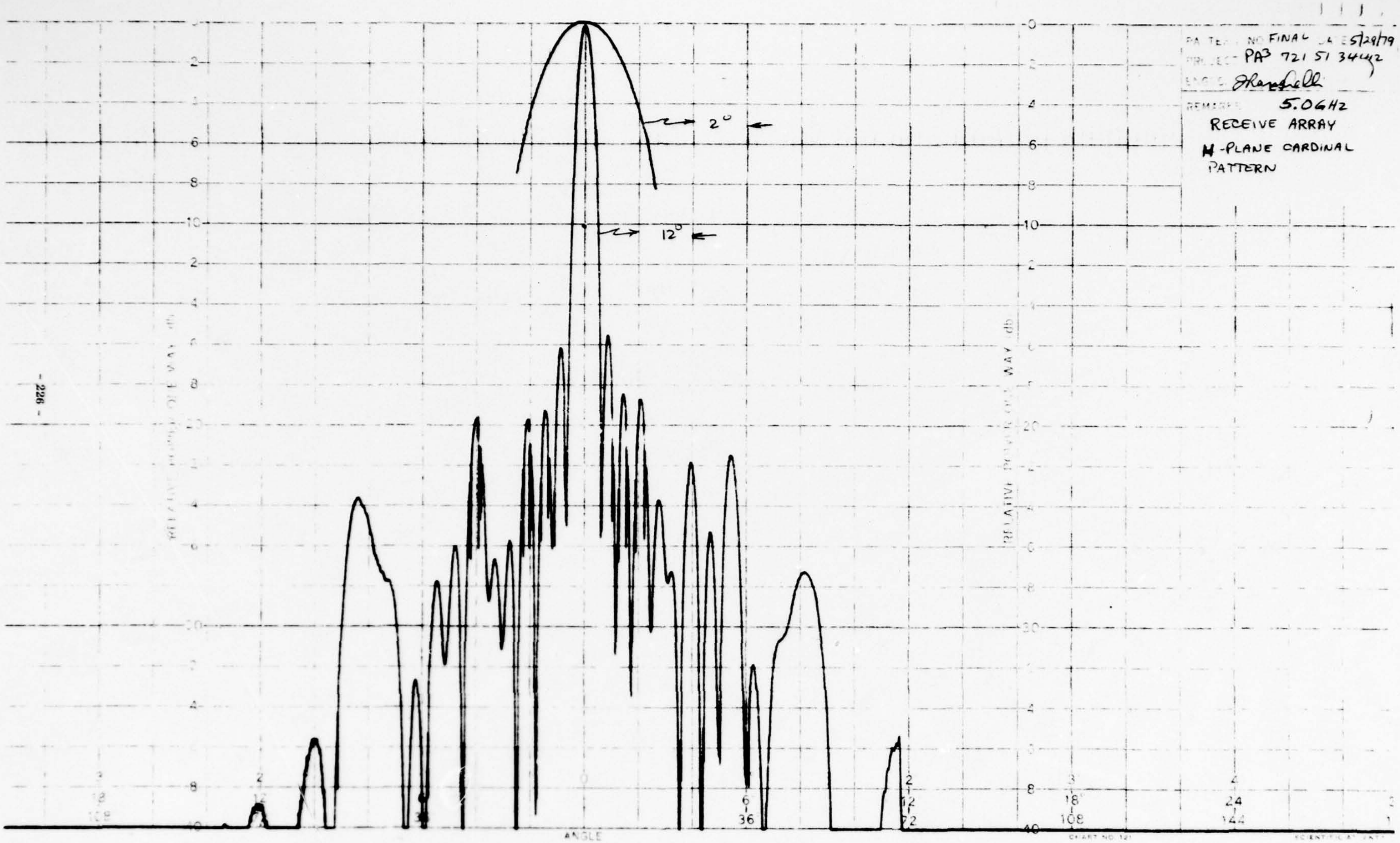

PATTERN NO FINAL DATE 5/21/79
PHASED ARRAY ANT.
PROJECT 721 51 4412
ENGRS J Runghelli
REMARKS
GAIN-RECEIVE
FREQ: GHz 5.00 4.95 4.90 4.85 4.80 4.75 4.70 4.65 4.60 4.55 4.50 4.45 4.40
ARRAY
SGH
MICROLAB
MOD # 638A
ARRAY-SGH: dB 10.6 9.9 10.0 10.4 10.8 11.2 10.1 9.7 12.0 12.4 11.5 11.0 11.0
SGH: dBi 18.65 18.60 18.55 18.5 18.4 18.3 18.25 18.2 18.15 18.10 18.00 17.95 17.90
TOTAL: dBi 29.25 28.50 28.55 28.9 29.2 29.5 28.35 27.9 30.15 30.50 29.5 28.95 28.90
ANGLE

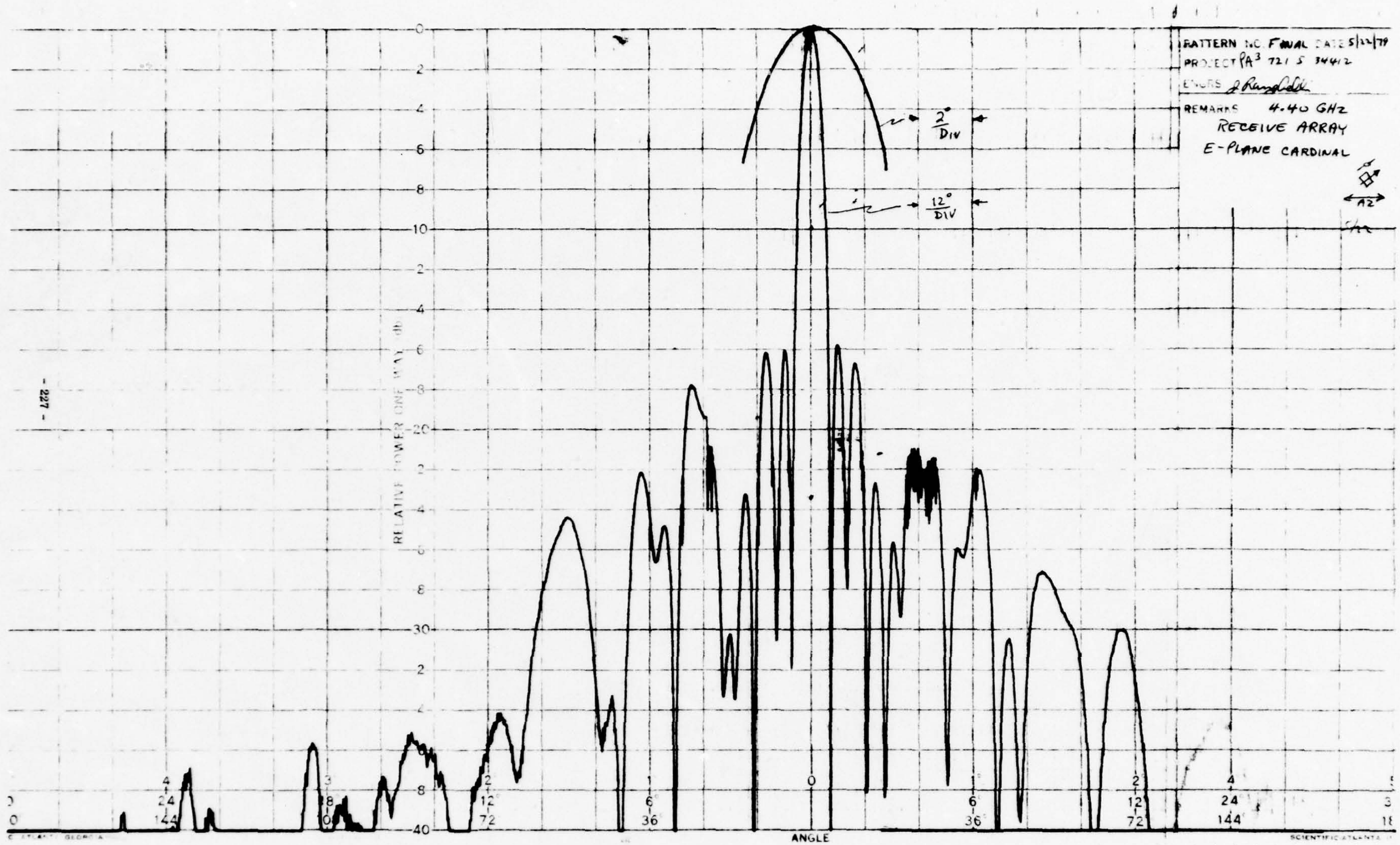

FINAL DATE 5/29/79
PA3 72-51 34412
4.4 GHz
RECEIVE ARRAY
H-PLANE CARDINAL
PATTERNS
2°
DIV
12°
DIV
RELATIVE POWER ONE WAY db
ANGLE

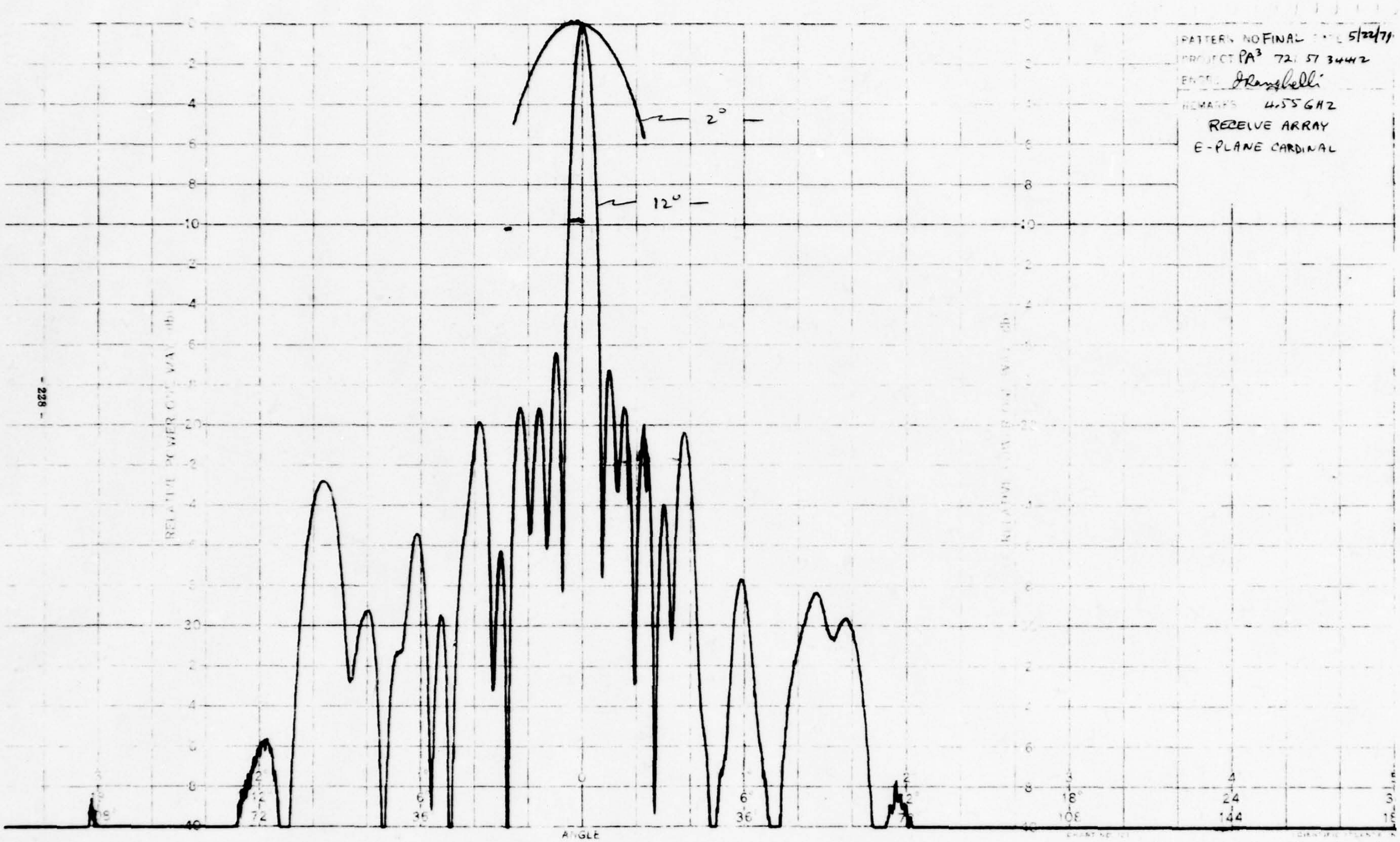

FINAL 5/29/79
PA3 771 51 34412
4.55GHz
RECEIVE ARRAY
H-PLANE CARDINAL PATTERN
2°
12°
ANGLE

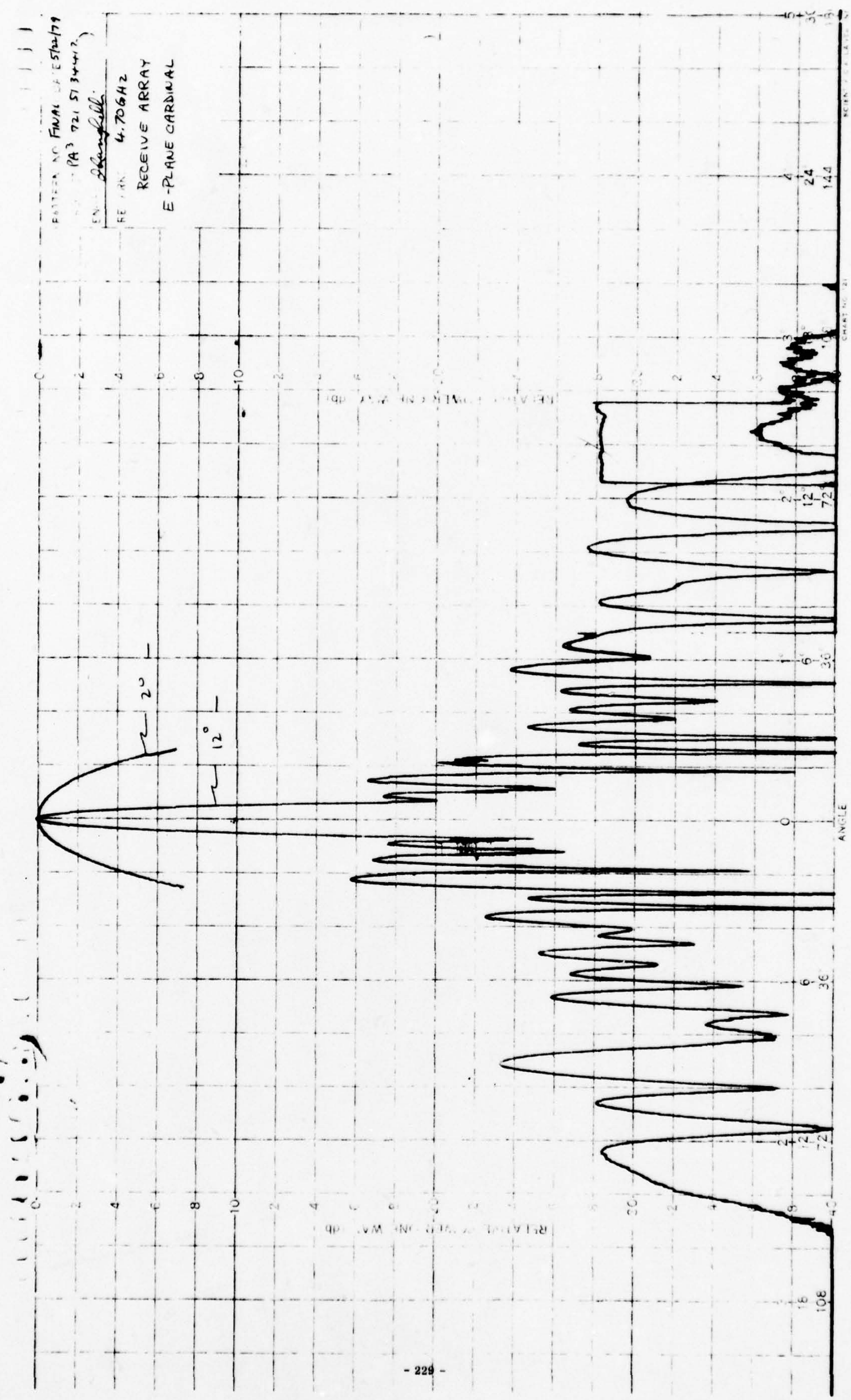

PATTERN NO FINAL 5/29/79
PROJECT PA3 51 54412
REMARKS 4.70 GHZ
RECEIVE ARRAY
H PLANE CARDINAL
PATTERN
2°
12°
ANGLE


PATTERN NO FINAL DATE 6/29/79
PROJECT PA3 721 51 3N412
ENGRS
REMARKS 4.85 GHZ
RECEIVE ARRAY
H-PLANE CARDINAL
PATTERN
2°
12°
RELATIVE POWER ONE WAY db
RELATIVE POWER ONE WAY db
ANGLE
0
6
36
12
72
18
108
24
144

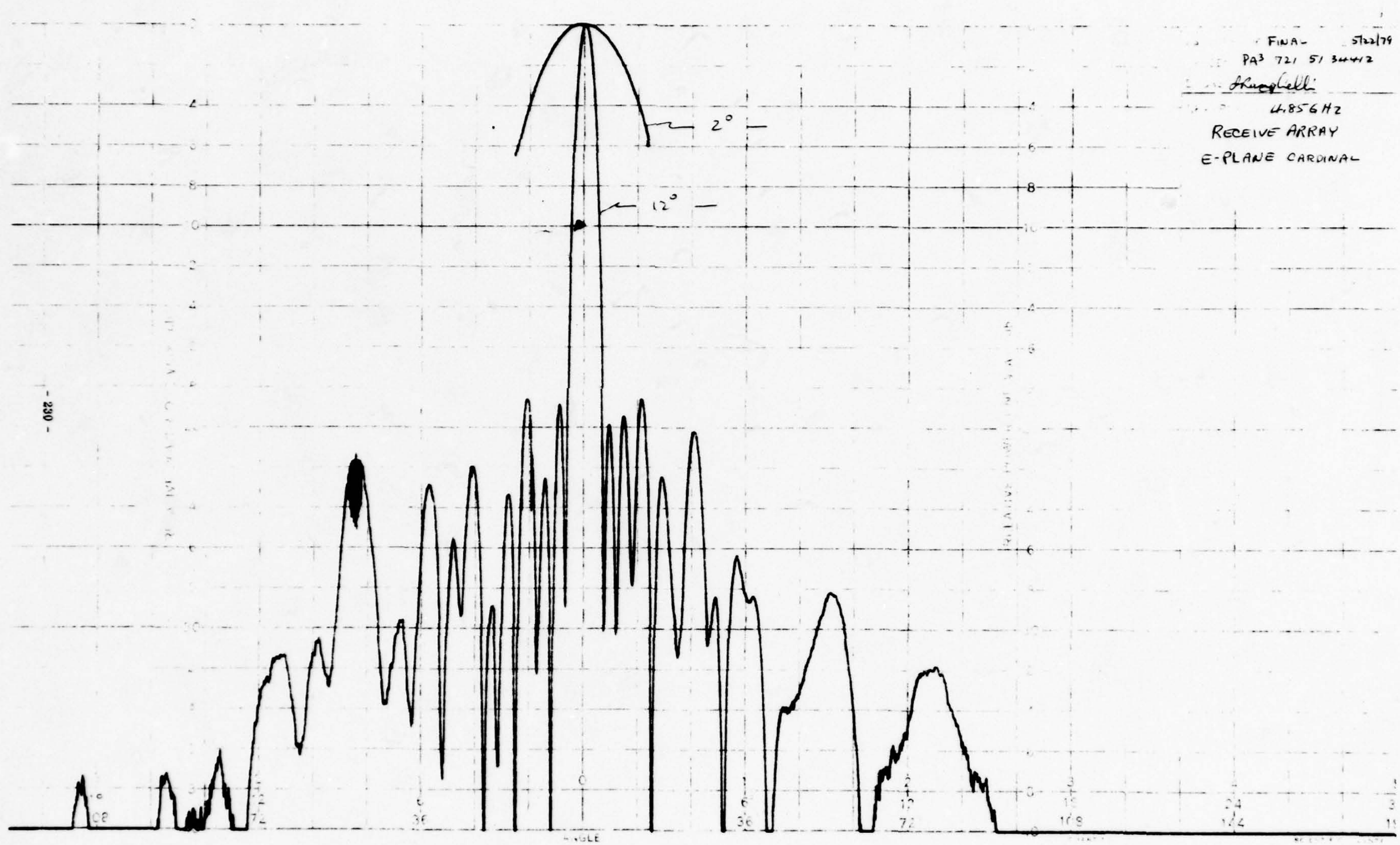

FINAL 5/28/79
PA3 721 51 34442
5.0GHz
RECEIVE ARRAY
H-PLANE CARDINAL
PATTERN
2°
12°
RELATIVE POWER OFF MAX (db)
ANGLE

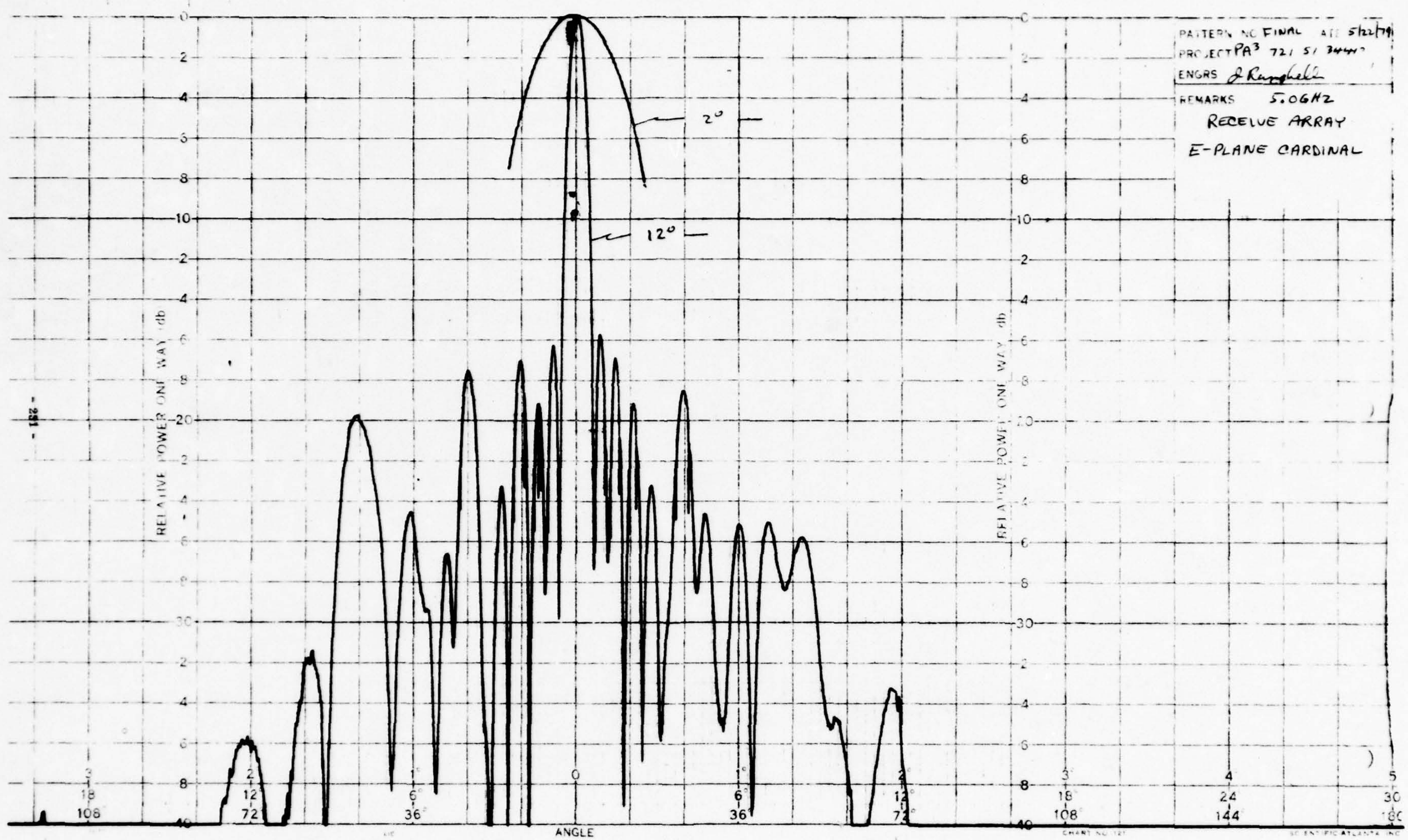

PATTERN NO. FINAL DATE 5/22/79
PROJECT PA³ 721 S 34412
ENGRS
REMARKS 4.40 GHz
RECEIVE ARRAY
E-PLANE CARDINAL
2°/DIV
12°/DIV
RELATIVE POWER ONE WAY (db)
ANGLE
SCIENTIFIC ATLANTA

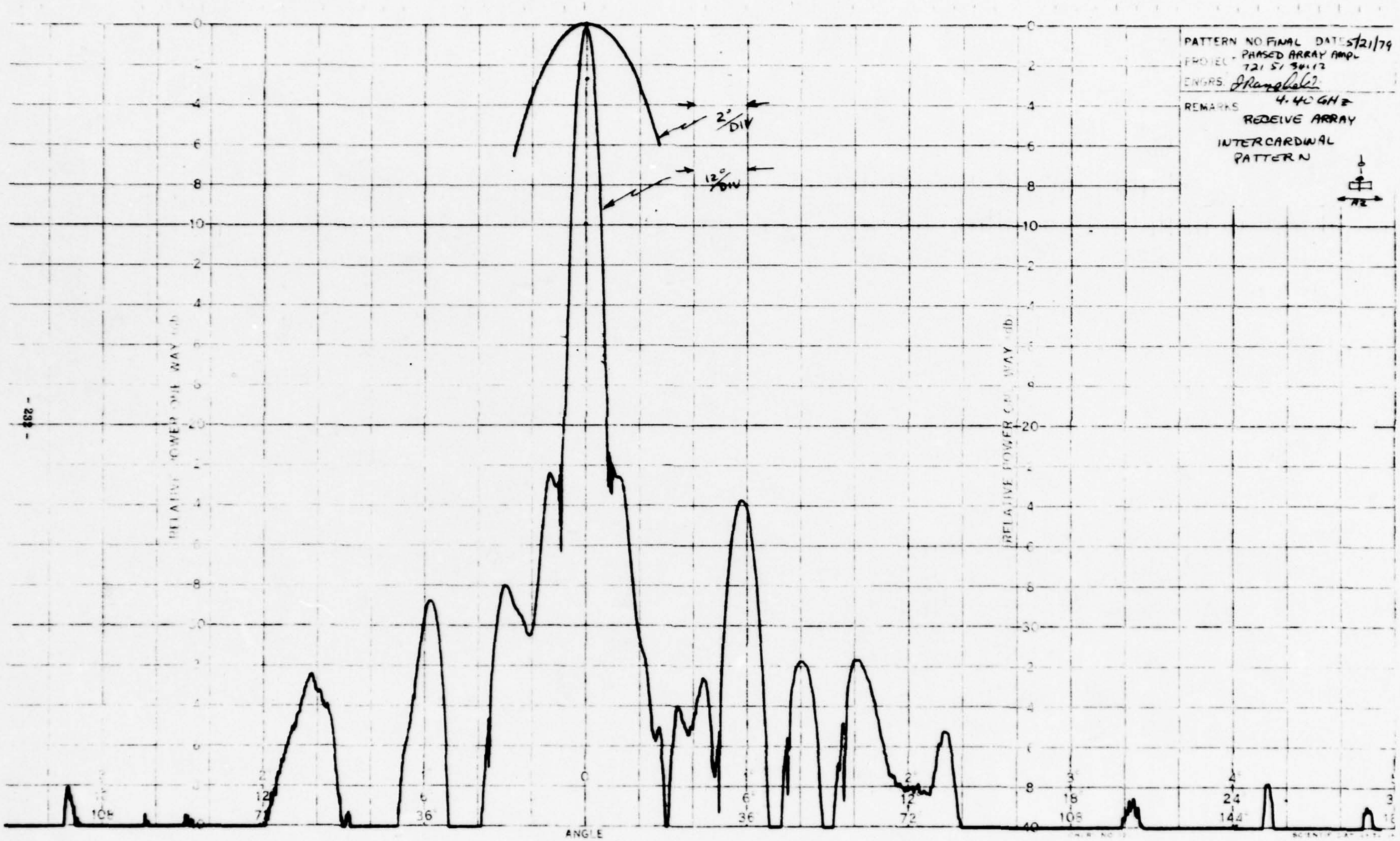

PATTERN NO FINAL 5/22/71
PROJECT PA³ 72 51 34412
ENGR. J. Rangibelli
REMARKS 4.55 GHZ
RECEIVE ARRAY
E-PLANE CARDINAL
2°
12°
ANGLE
RELATIVE POWER OFF MAX (dB)

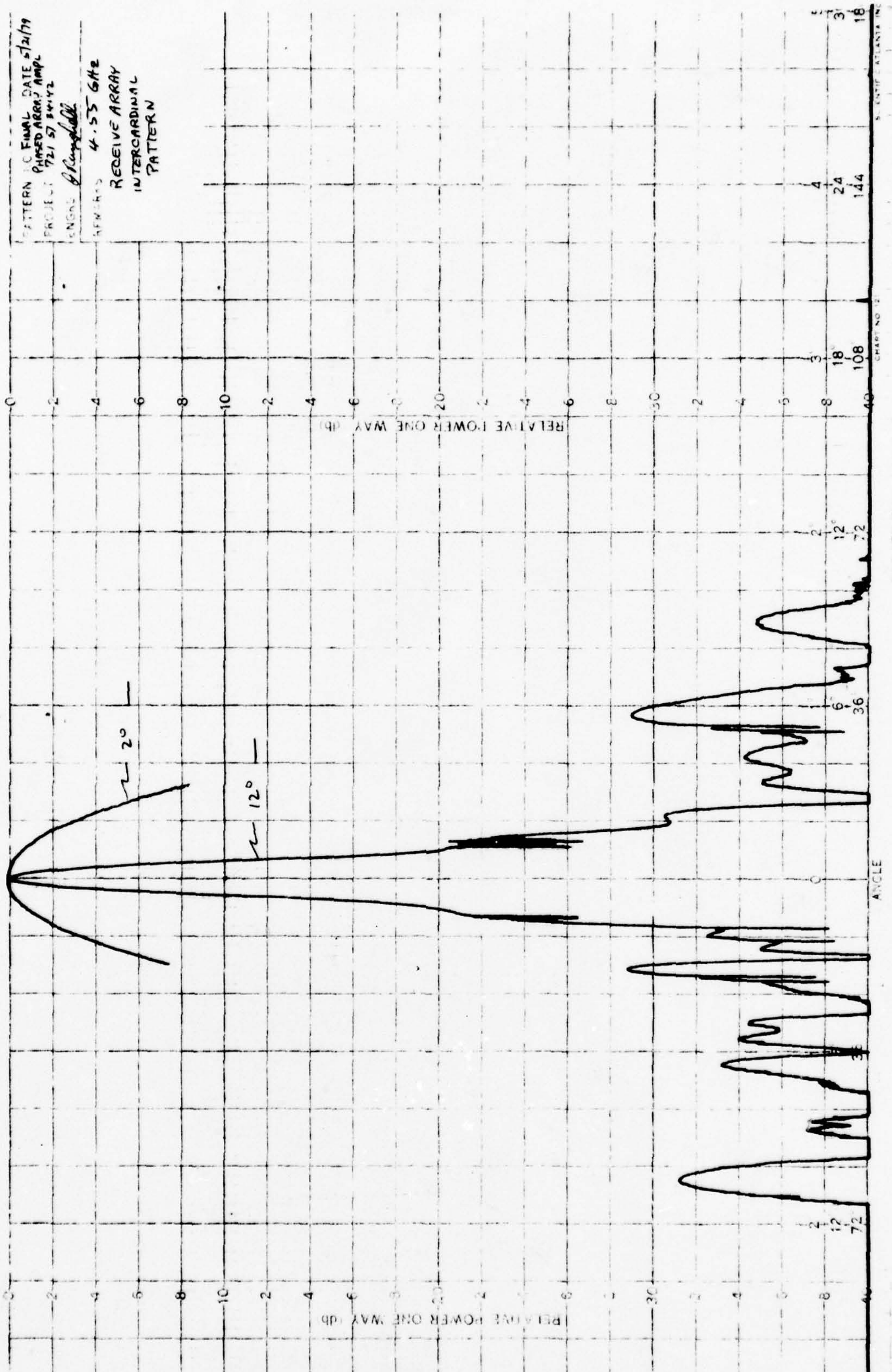


4.70GHz
RECEIVE ARRAY
E-PLANE CARDINAL
2°
12°
ANGLE

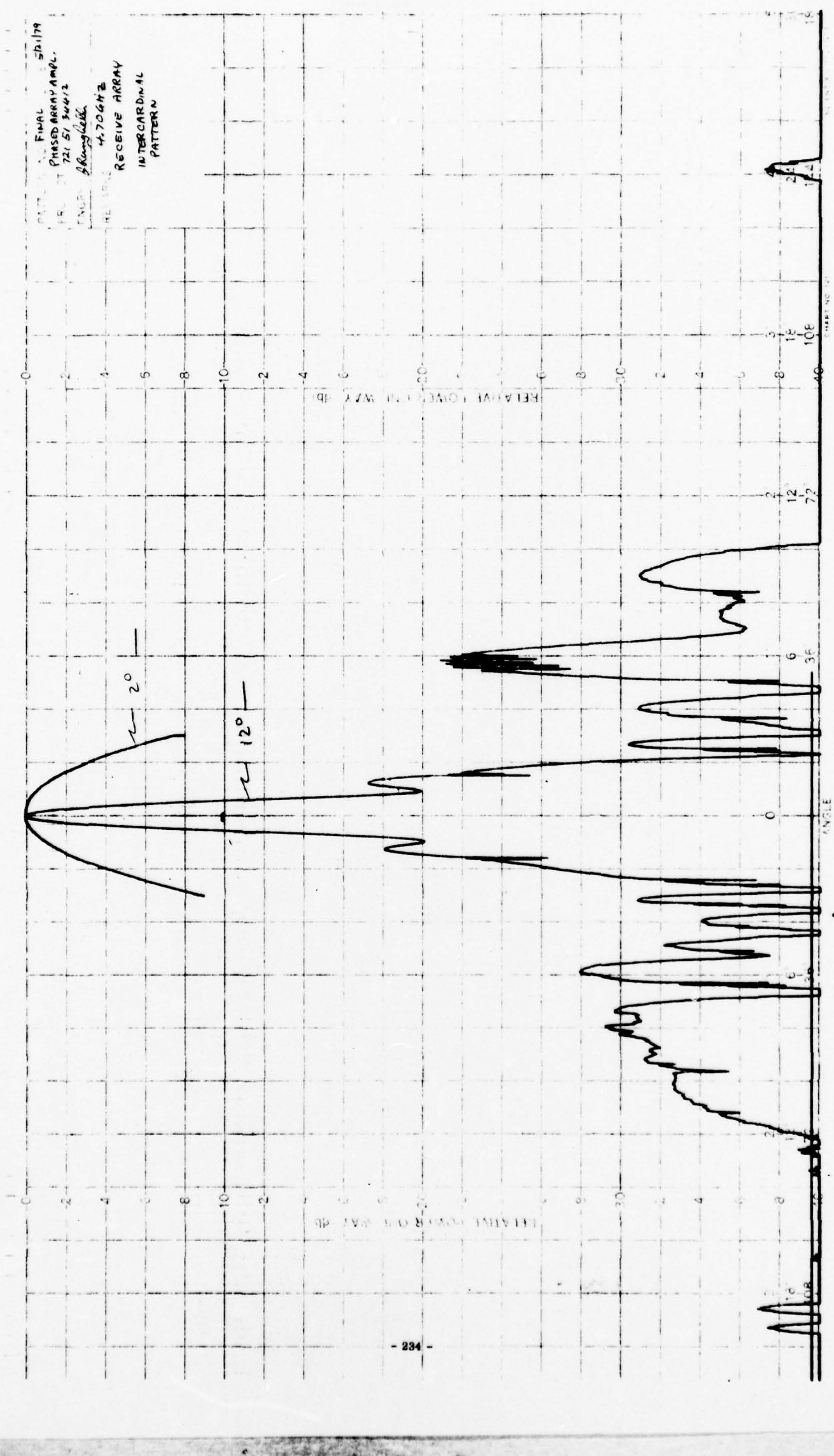

FINAL 5/22/79
4.85GHz
RECEIVE ARRAY
E-PLANE CARDINAL
2°
12°
ANGLE


PATTERN NO FINAL
PROJECT PA³ 721 51 344
ENGRS J Rumpbell
REMARKS 5.0GHz
RECEIVE ARRAY
E-PLANE CARDINAL
2°
12°
RELATIVE POWER ONE WAY db
ANGLE

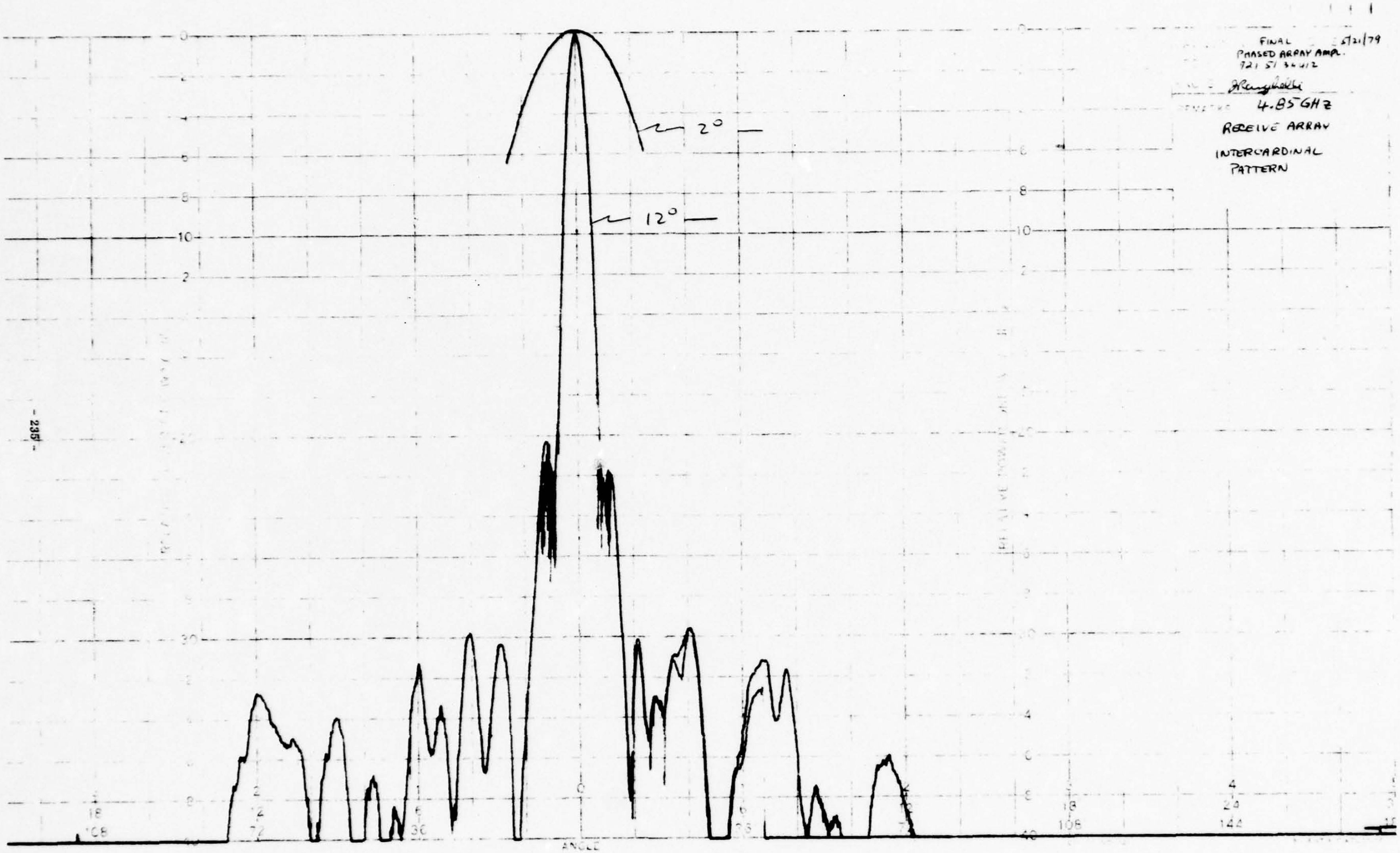

PATTERN NO FINAL DATE 5/21/79
PROJECT - PHASED ARRAY AMPL 721 51 34112
ENGRS.
REMARKS 4.40 GHz
RECEIVE ARRAY
INTERCARDINAL PATTERN
AZ
2°/DIV
12°/DIV
RELATIVE POWER ONE WAY (db)
ANGLE
0
2
4
6
8
10
20
30
40
12
72
36
18
108
24
144

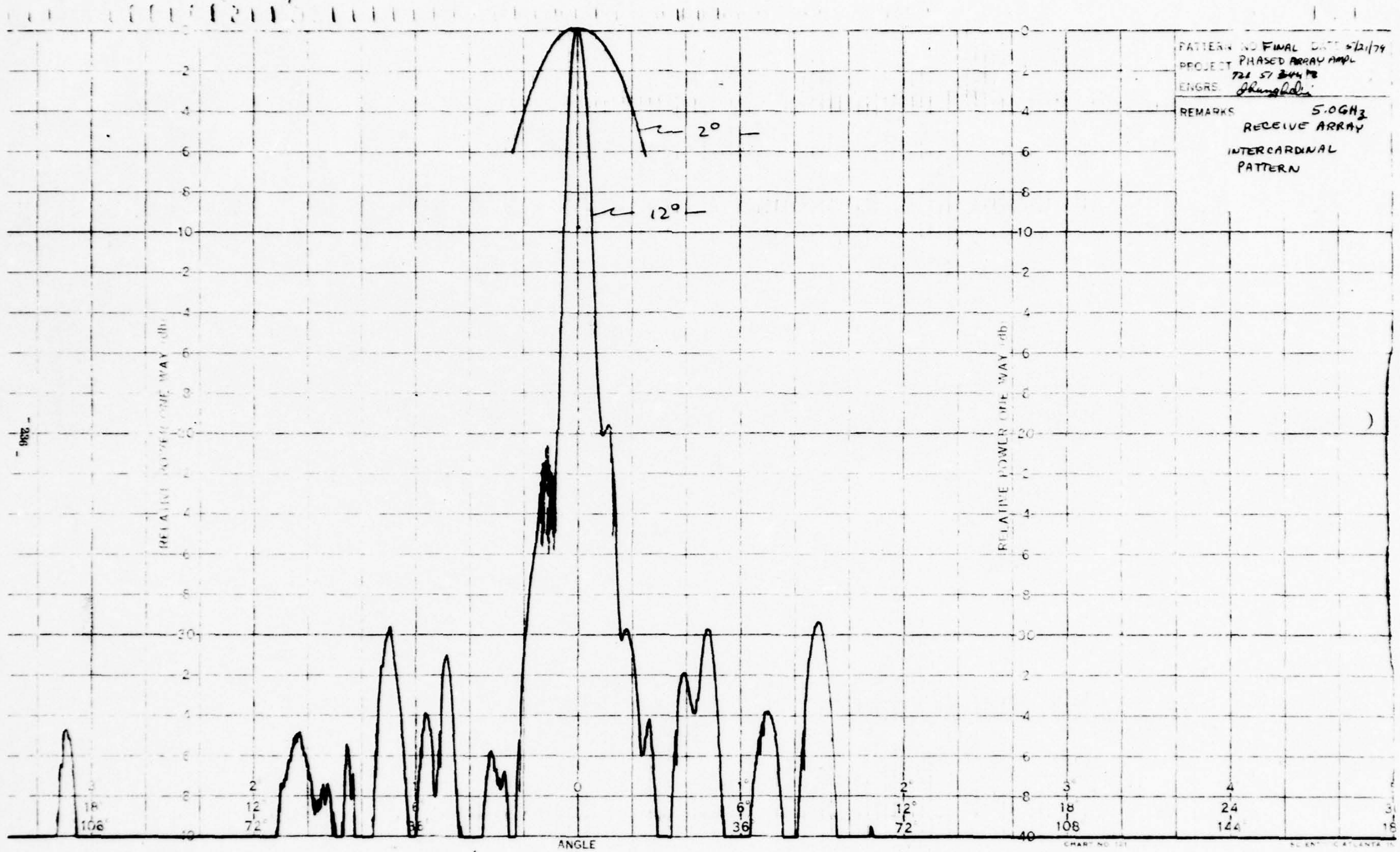


PATTERN NO. FINAL
DATE 5/21/79
PHASED ARRAY AMPL
4.55 GHz
RECEIVE ARRAY
INTERCARDINAL
PATTERN
RELATIVE POWER ONE WAY (db)
ANGLE
2°
12°



FINAL
PHASED ARRAY AMPL.
721 51 34412
4.70GHz
RECEIVE ARRAY
INTERCARDINAL
PATTERN
2°
12°
ANGLE

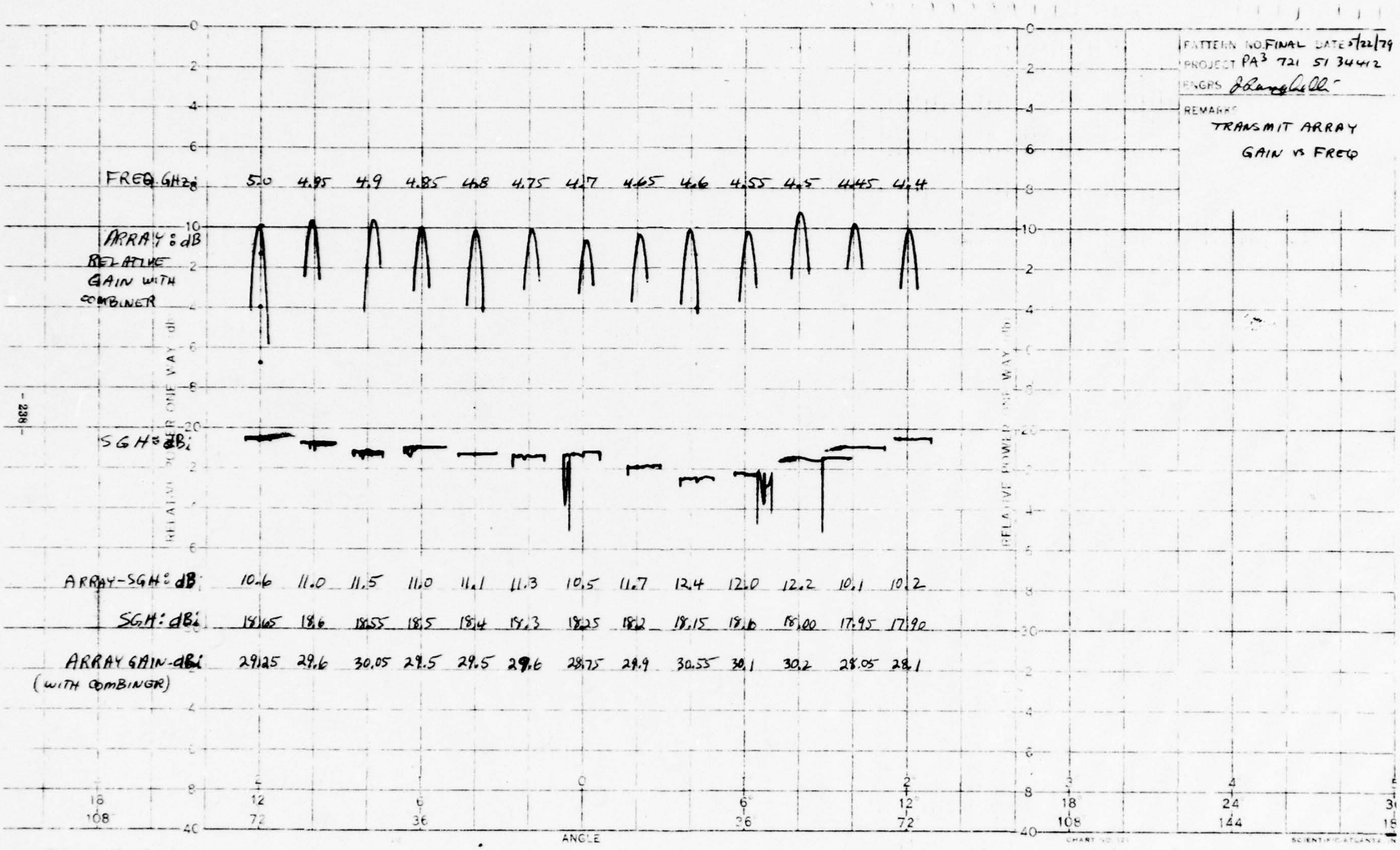

FINAL 5/21/79
PHASED ARRAY AMP.
721 51 34412
4.85 GHz
RECEIVE ARRAY
INTERCARDINAL
PATTERN
2°
12°
ANGLE

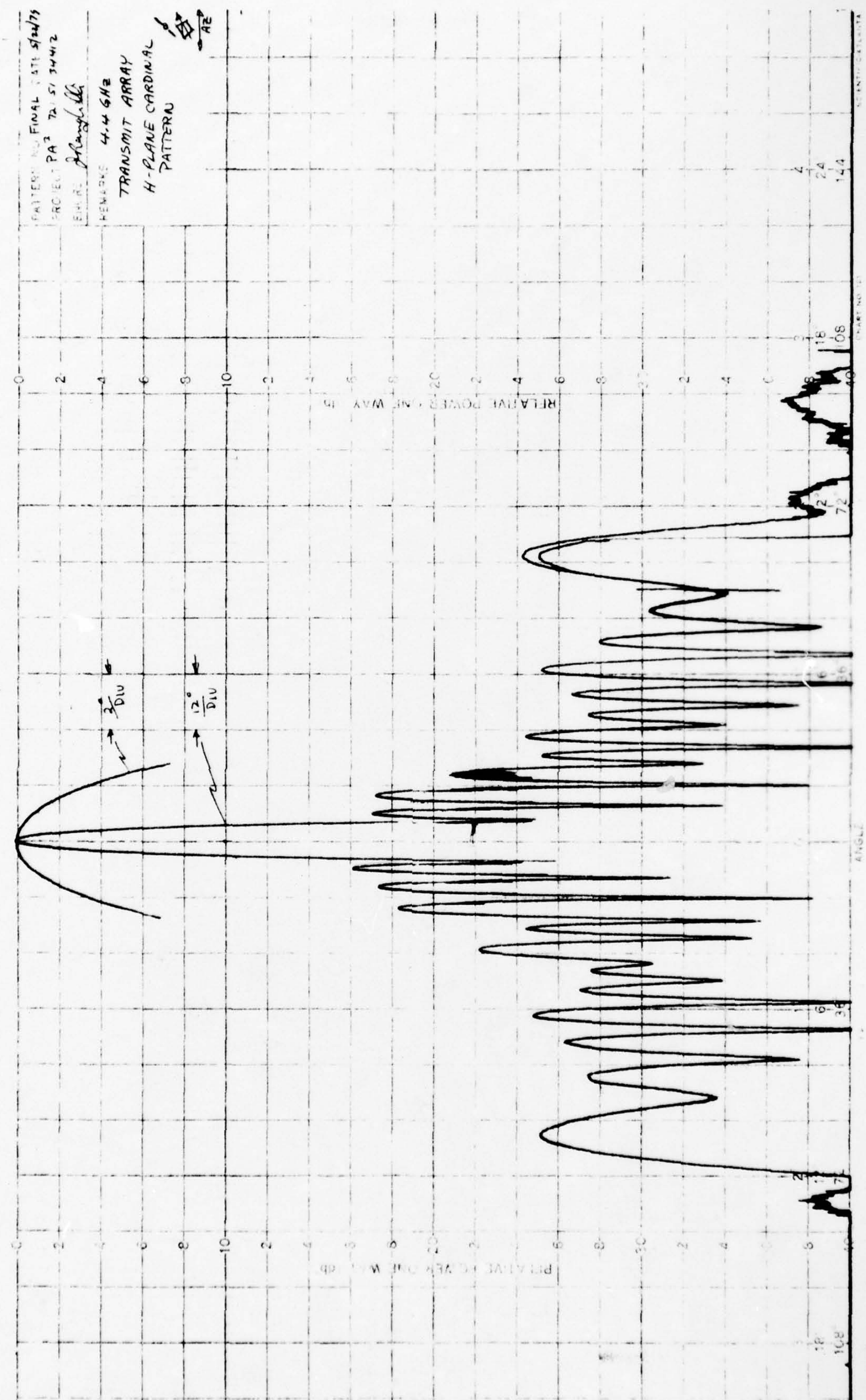

PATTERN NO FINAL DATE 5/21/74
PROJECT PHASED ARRAY AMPL 721 57 344 78
ENGRS
REMARKS 5.0GHz
RECEIVE ARRAY
INTERCARDINAL PATTERN
2°
12°
RELATIVE POWER ONE WAY (db)
ANGLE

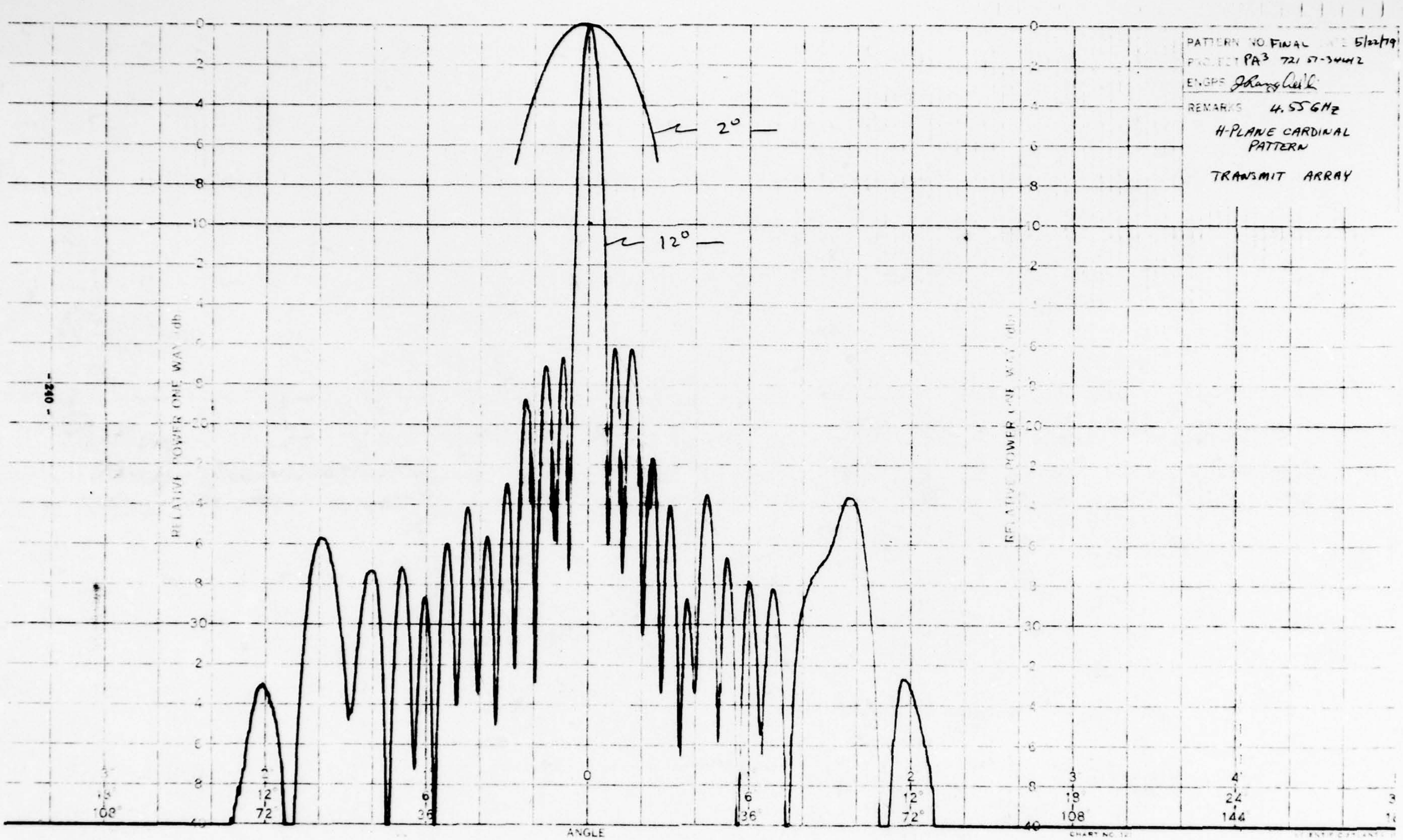
ANTENNA GAIN AND SIDELOBE PATTERNS
TRANSMIT ARRAY

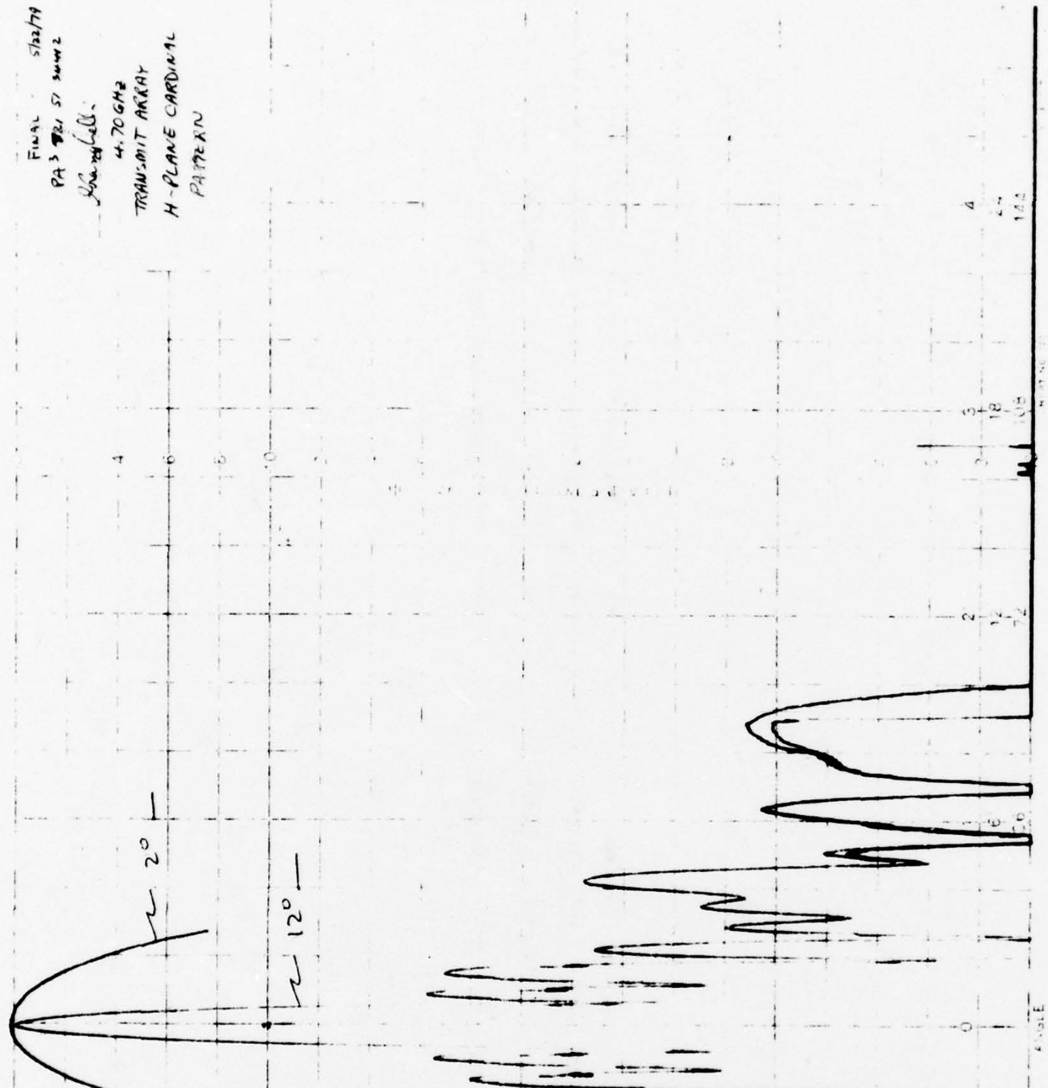
- Assembled in Final Configuration less the G10 Epoxy Fiber Glass Radome

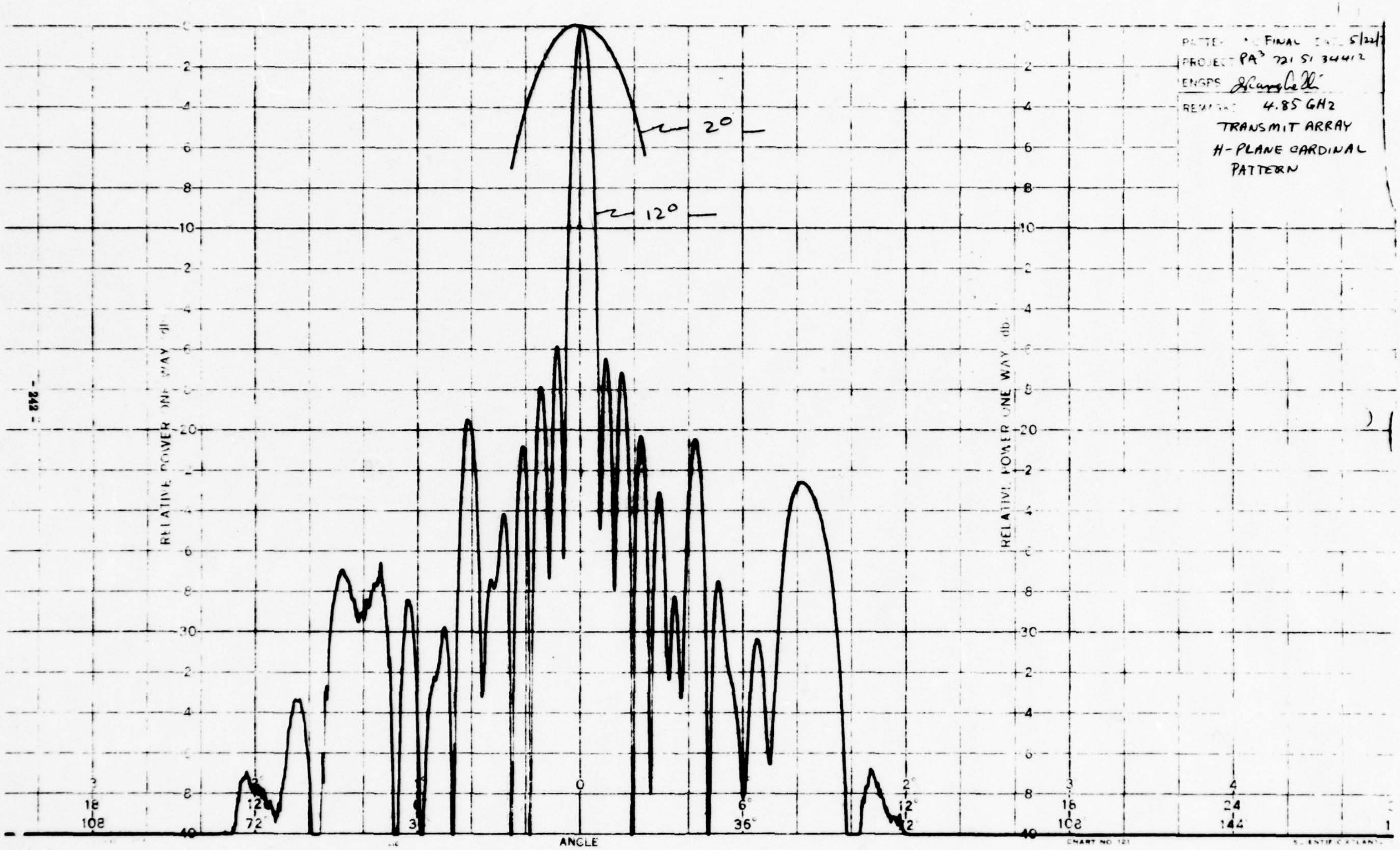
Gain	13 Frequencies
Sidelobes	
H Plane	1 Frequency/Pattern
E Plane	5 Patterns each plane
Intercardinial Plane	(4.4, 4.55, 4.7, 4.85, 5.0 GHz)

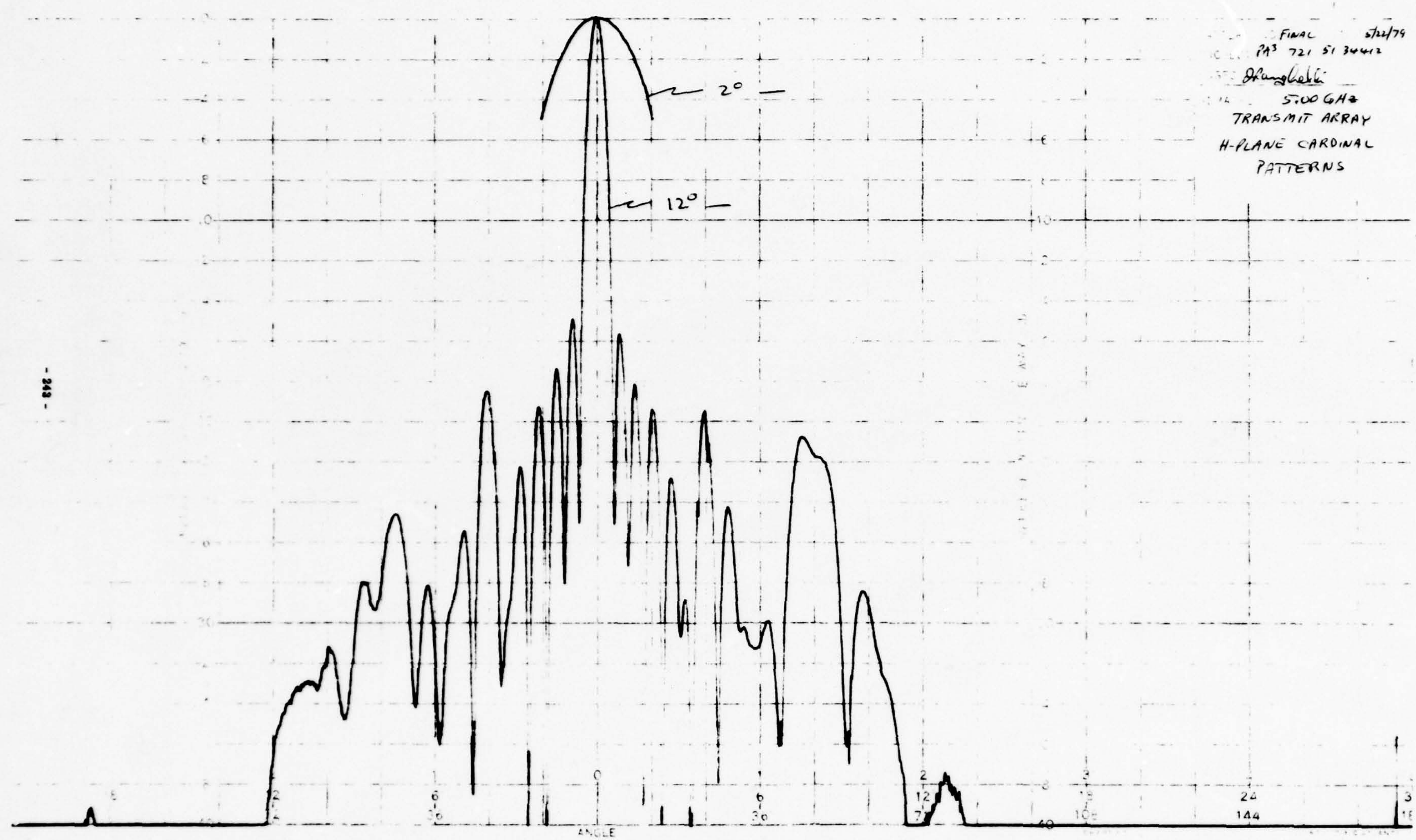

PATTERN NO. FINAL DATE 5/22/79
PROJECT PA3 721 51 34412
ENGRS
REMARKS
TRANSMIT ARRAY
GAIN vs FREQ
FREQ GHz: 5.0 4.95 4.9 4.85 4.8 4.75 4.7 4.65 4.6 4.55 4.5 4.45 4.4
ARRAY: dB
RELATIVE GAIN WITH COMBINER
SGH: dBi
ARRAY-SGH: dB 10.6 11.0 11.5 11.0 11.1 11.3 10.5 11.7 12.4 12.0 12.2 10.1 10.2
SGH: dBi 18.65 18.6 18.55 18.5 18.4 18.3 18.25 18.2 18.15 18.1 18.00 17.95 17.90
ARRAY GAIN-dBi (WITH COMBINER) 29.25 29.6 30.05 29.5 29.5 29.6 28.75 29.9 30.55 30.1 30.2 28.05 28.1
RELATIVE POWER ONE WAY dB
ANGLE
CHART NO.
SCIENTIFIC ATLANTA INC

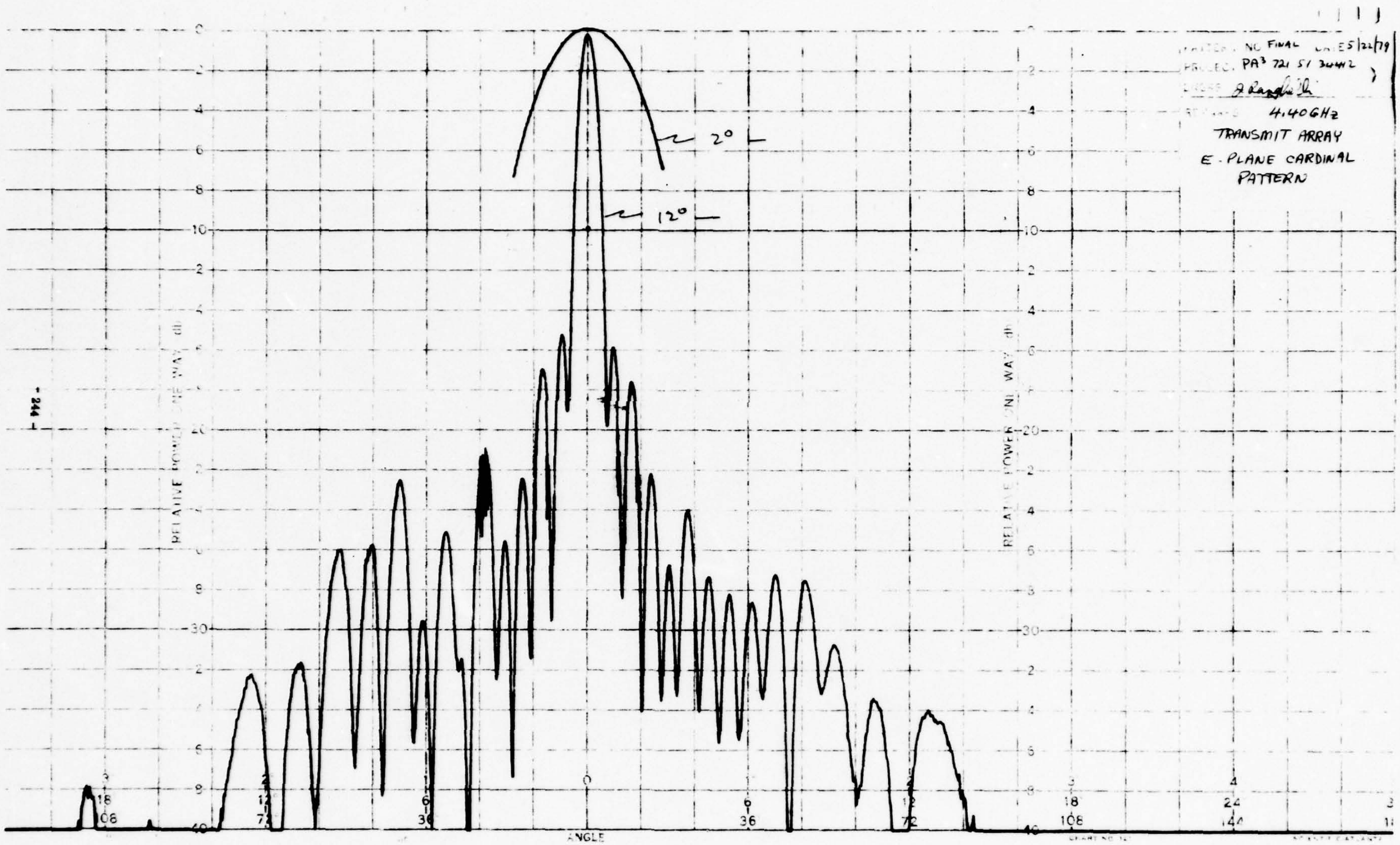

PATTERN NO FINAL DATE 5/24/75
PROJECT PA² 72 51 34412
REMARKS 4.4 GHz
TRANSMIT ARRAY
H-PLANE CARDINAL PATTERN
AZ
3°/DIV
12°/DIV
RELATIVE POWER ONE WAY db
ANGLE
CHART NO.
SCIENTIFIC ATLANTA


PATTERN NO FINAL
5/22/79
PROJECT PA³ 721 57-3442
REMARKS 4.55 GHz
H-PLANE CARDINAL PATTERN
TRANSMIT ARRAY
2°
12°
RELATIVE POWER ONE WAY (db)
ANGLE
0
2
4
6
8
10
20
30
40
12°
72°
36
108
144

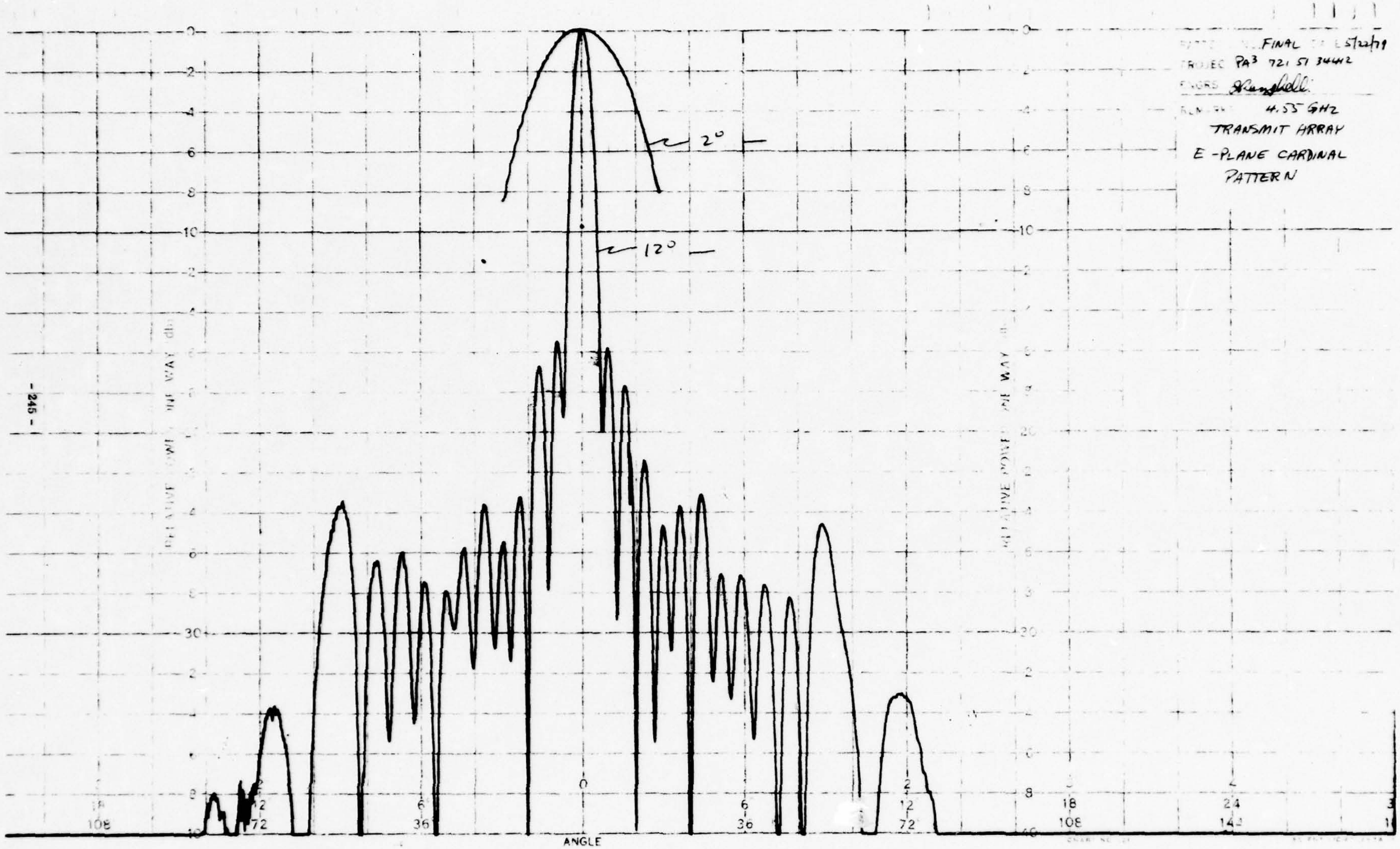

FINAL 5/22/79
4.70 GHz
TRANSMIT ARRAY
H-PLANE CARDINAL
PATTERN
2°
12°
ANGLE

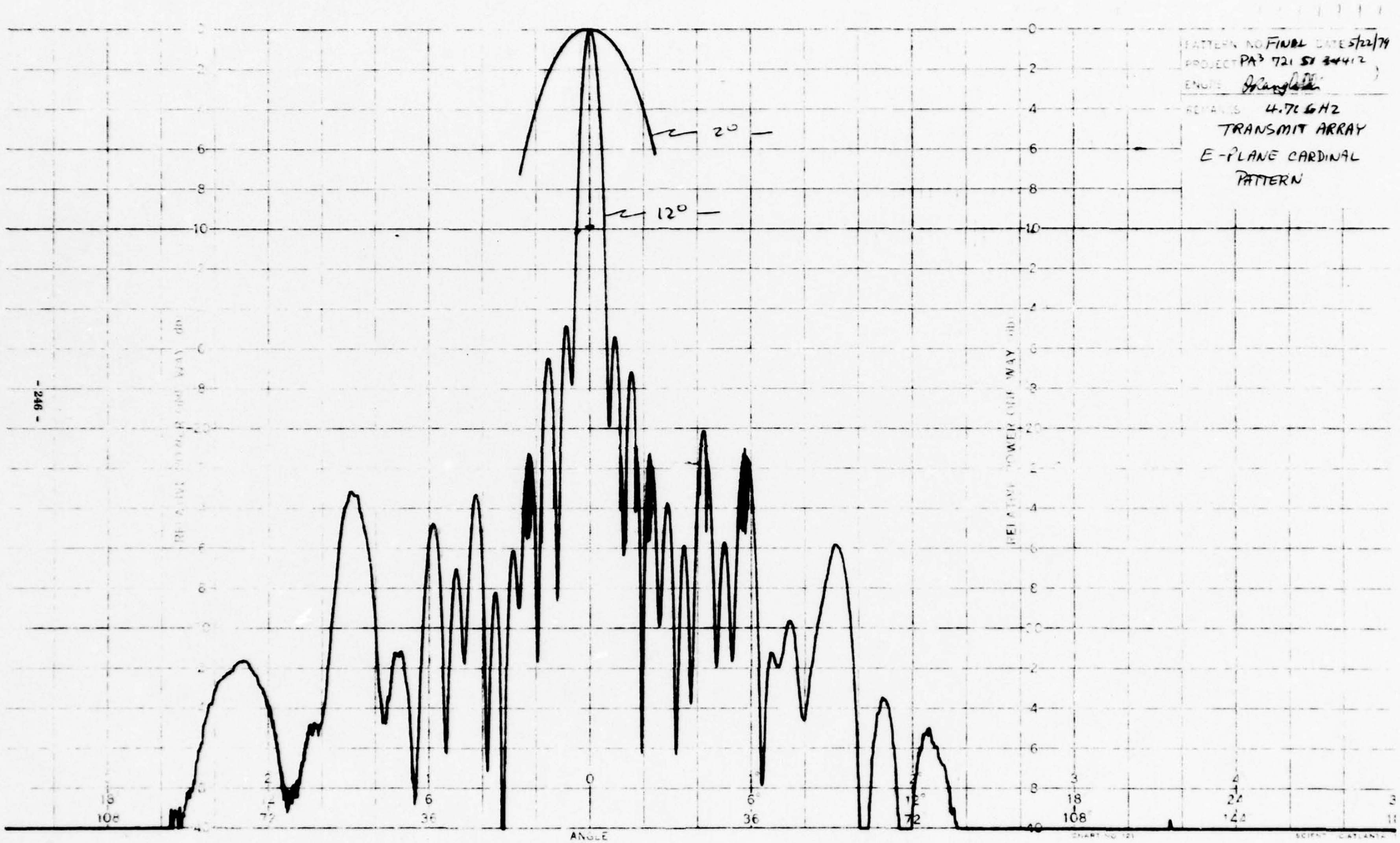

FINAL DATE 5/22/
PROJECT PA³ 721 51 34412
ENGRS
REMARKS 4.85 GHz
TRANSMIT ARRAY
H-PLANE CARDINAL
PATTERN
20°
120°
RELATIVE POWER ONE WAY db
ANGLE
CHART NO 121

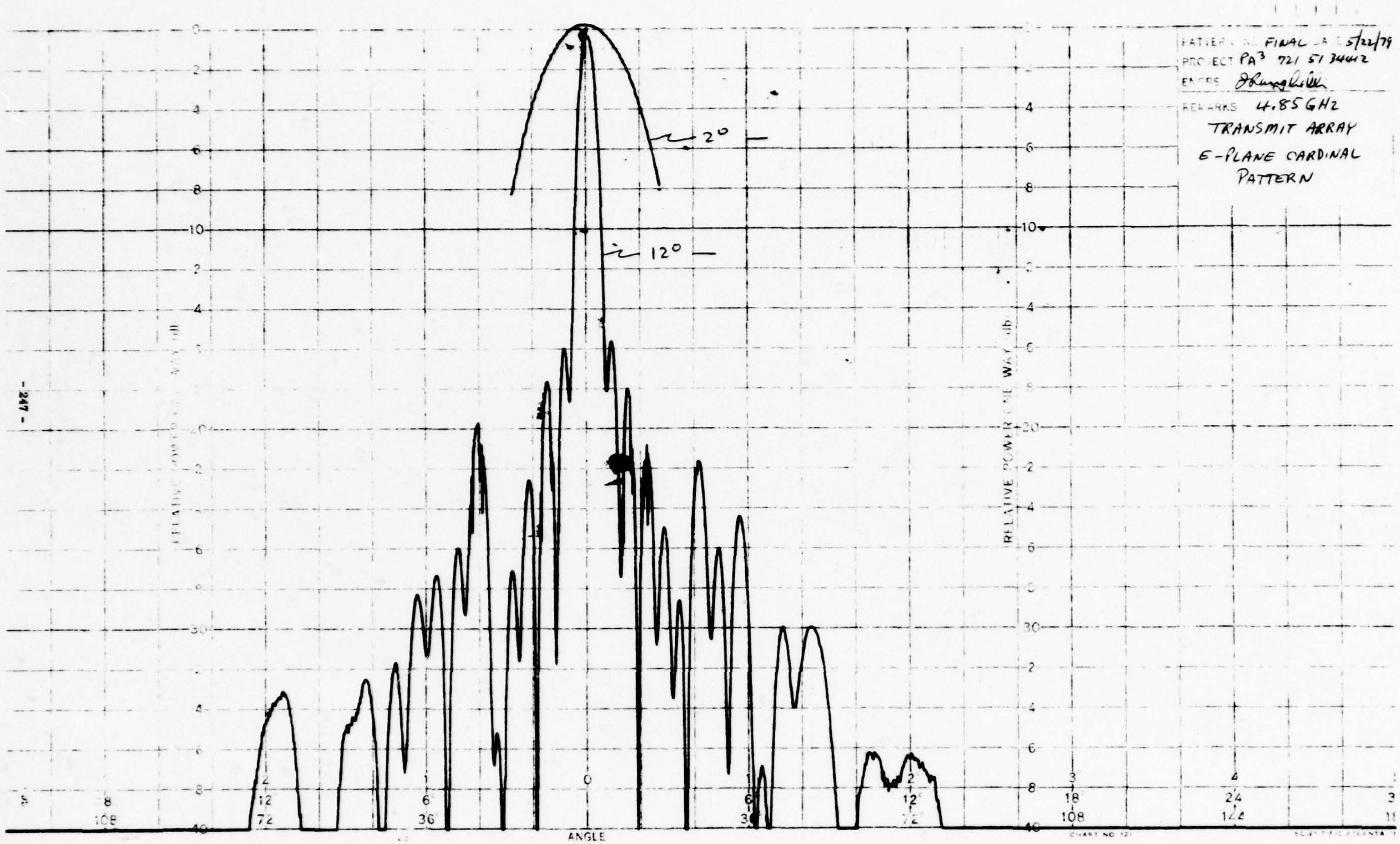

FINAL 5/22/79
PA3 721 51 34412
5.00 GHz
TRANSMIT ARRAY
H-PLANE CARDINAL
PATTERNS
2°
12°
ANGLE



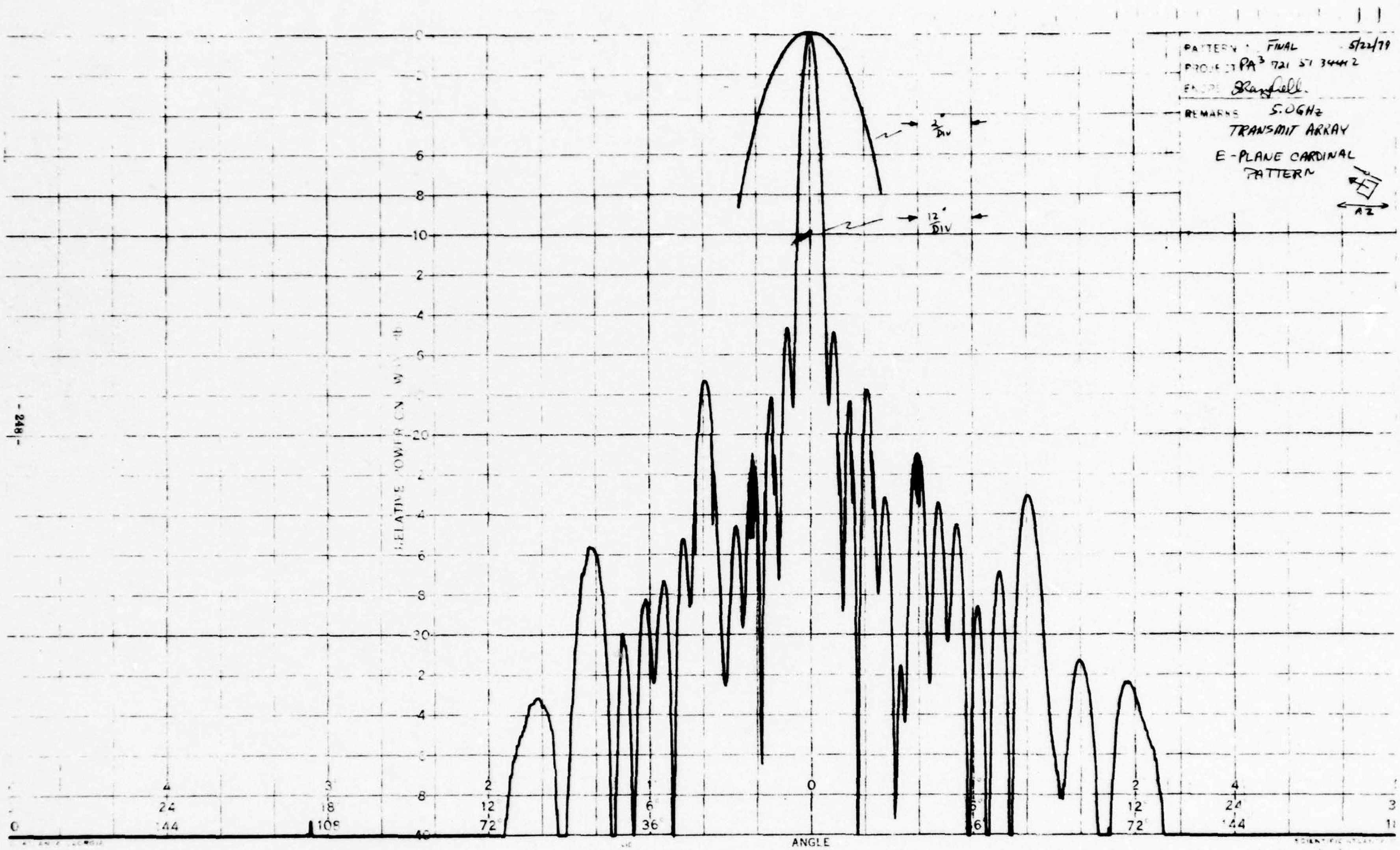
PATTERN NO FINAL DATE 5/22/79
PROJECT PA3 721 51 3uuu2
4.40GHz
TRANSMIT ARRAY
E-PLANE CARDINAL PATTERN
2°
12°
RELATIVE POWER ONE WAY db
ANGLE

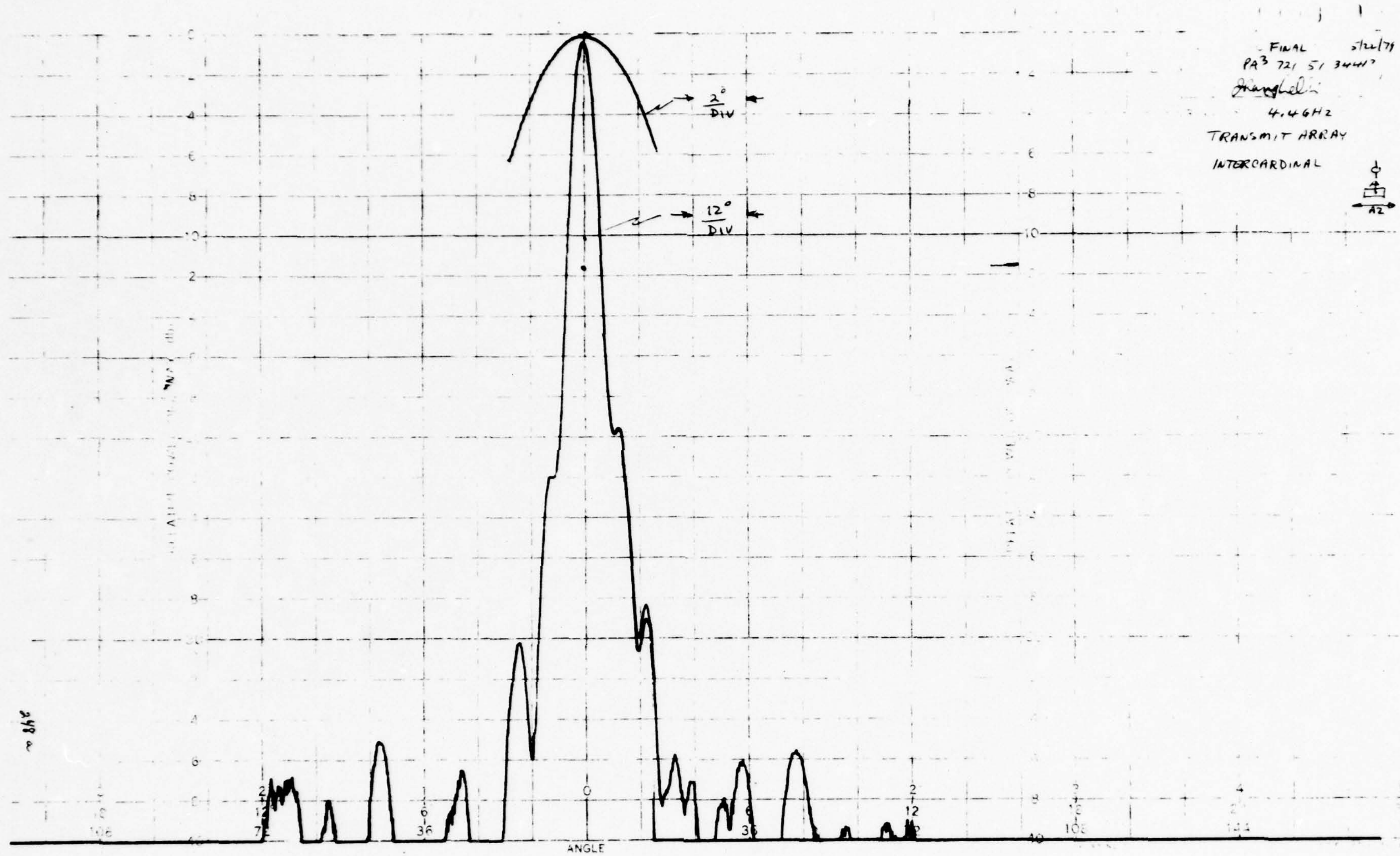

FINAL 5/22/79
PA3 721 51 344412
4.55 GHz
TRANSMIT ARRAY
E-PLANE CARDINAL
PATTERN
2°
12°
ANGLE
RELATIVE POWER ONE WAY dB


PATTERN NO FINAL DATE 5/22/79
PROJECT PA3 721 51 34412
REMARKS 4.76 GHZ
TRANSMIT ARRAY
E-PLANE CARDINAL
PATTERN
2°
12°
RELATIVE POWER ONE WAY db
ANGLE
0
6
36
72
108
144



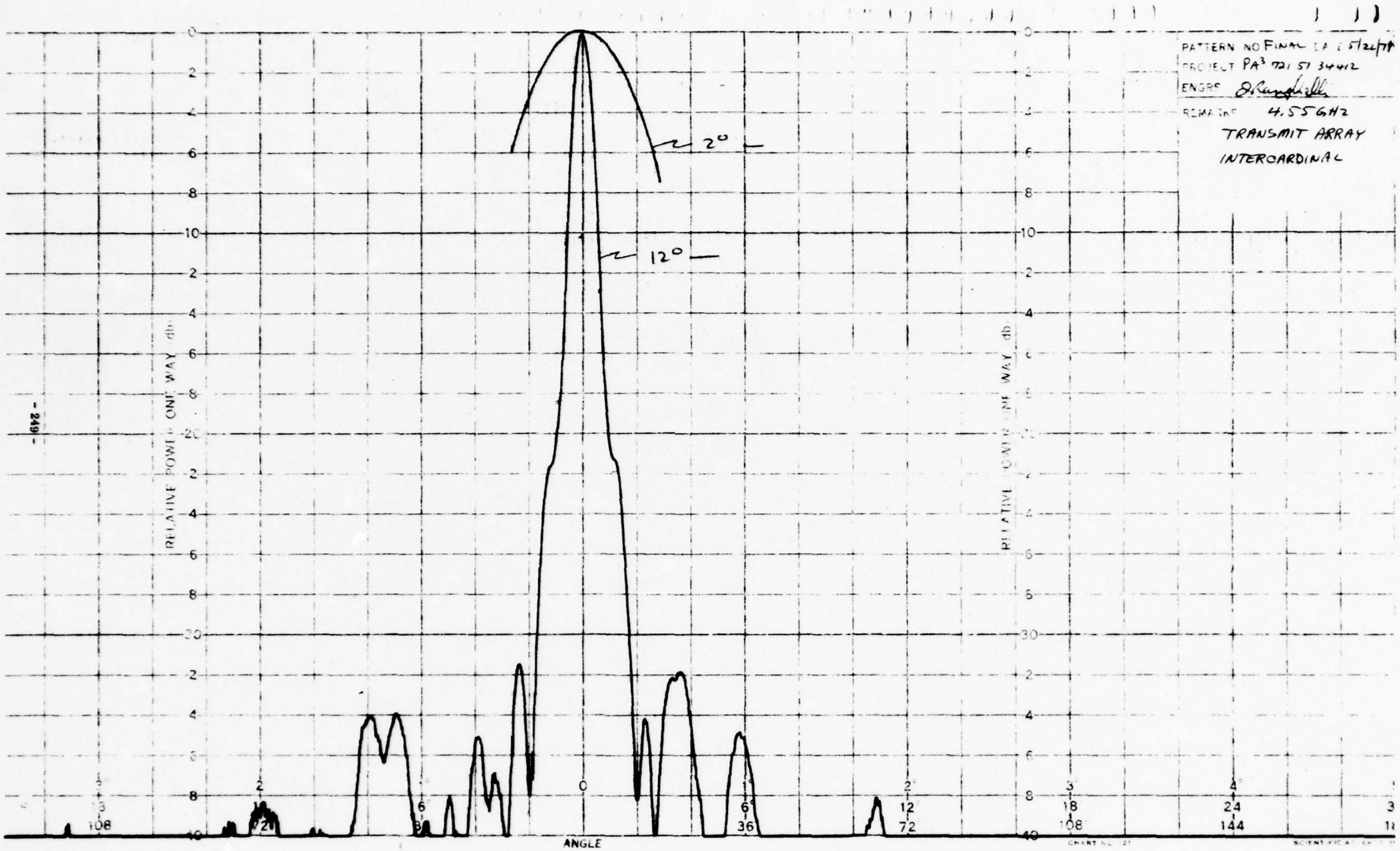
PATTERN NO. FINAL DATE 5/22/79
PROJECT PA³ 721 51 34412
REMARKS 4.85 GHz
TRANSMIT ARRAY
E-PLANE CARDINAL
PATTERN
2°
12°
RELATIVE POWER ONE WAY db
ANGLE
CHART NO 121

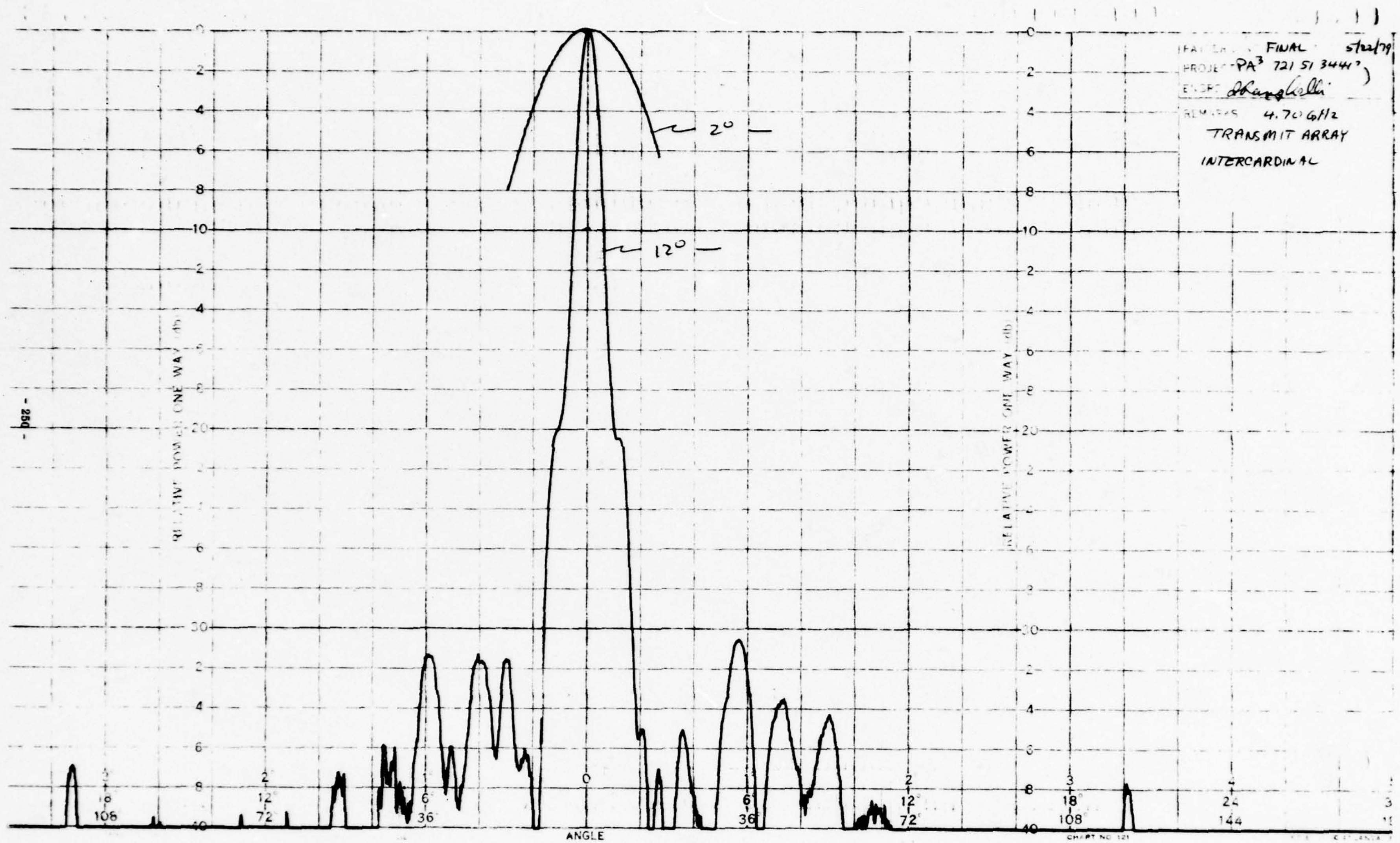

PATTERN FINAL 5/22/79
PROJECT PA³ 721 57 3444 2
REMARKS 5.0GHz
TRANSMIT ARRAY
E-PLANE CARDINAL
PATTERN
AZ
2°/DIV
12°/DIV
RELATIVE POWER CN ... dB
ANGLE

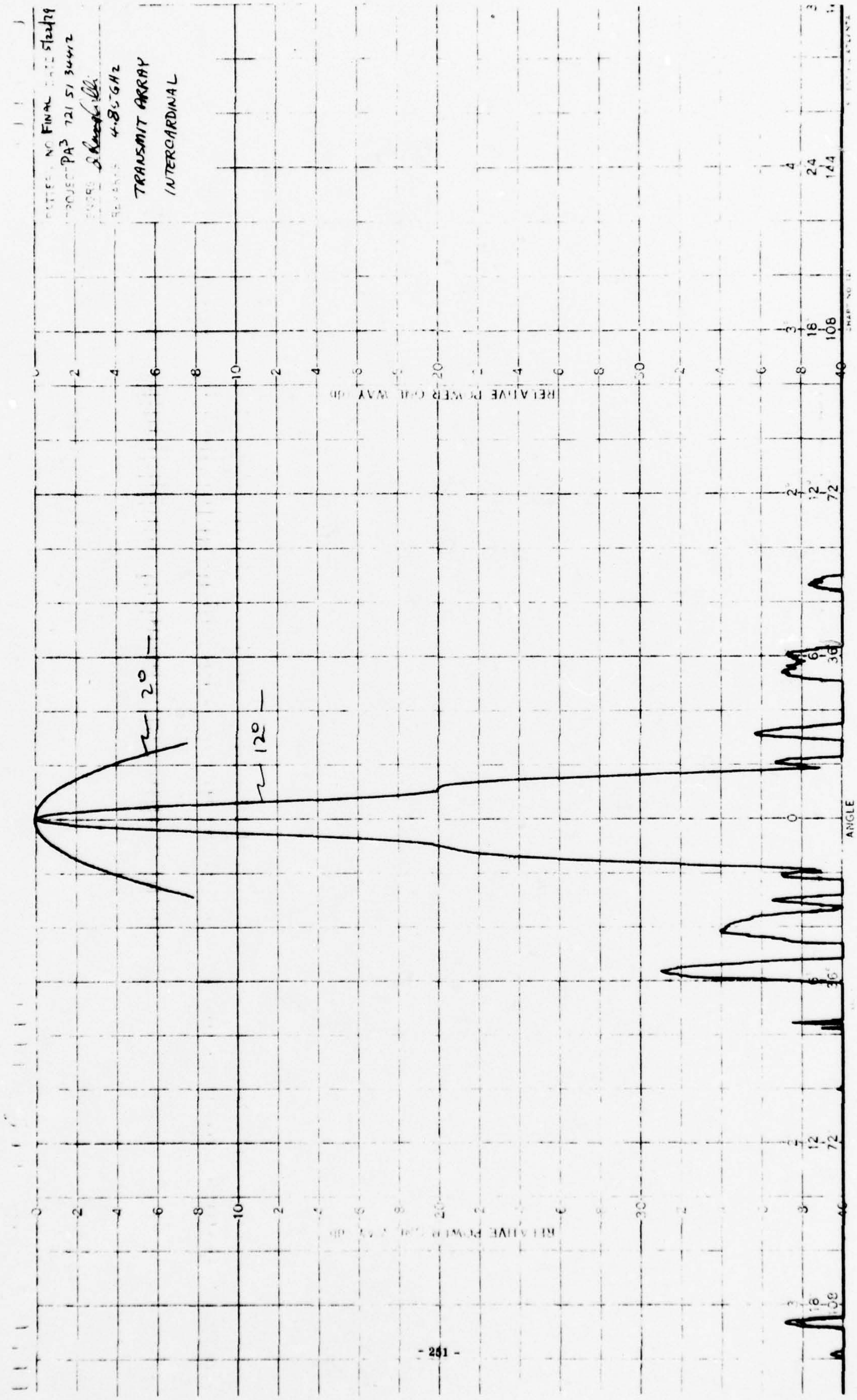


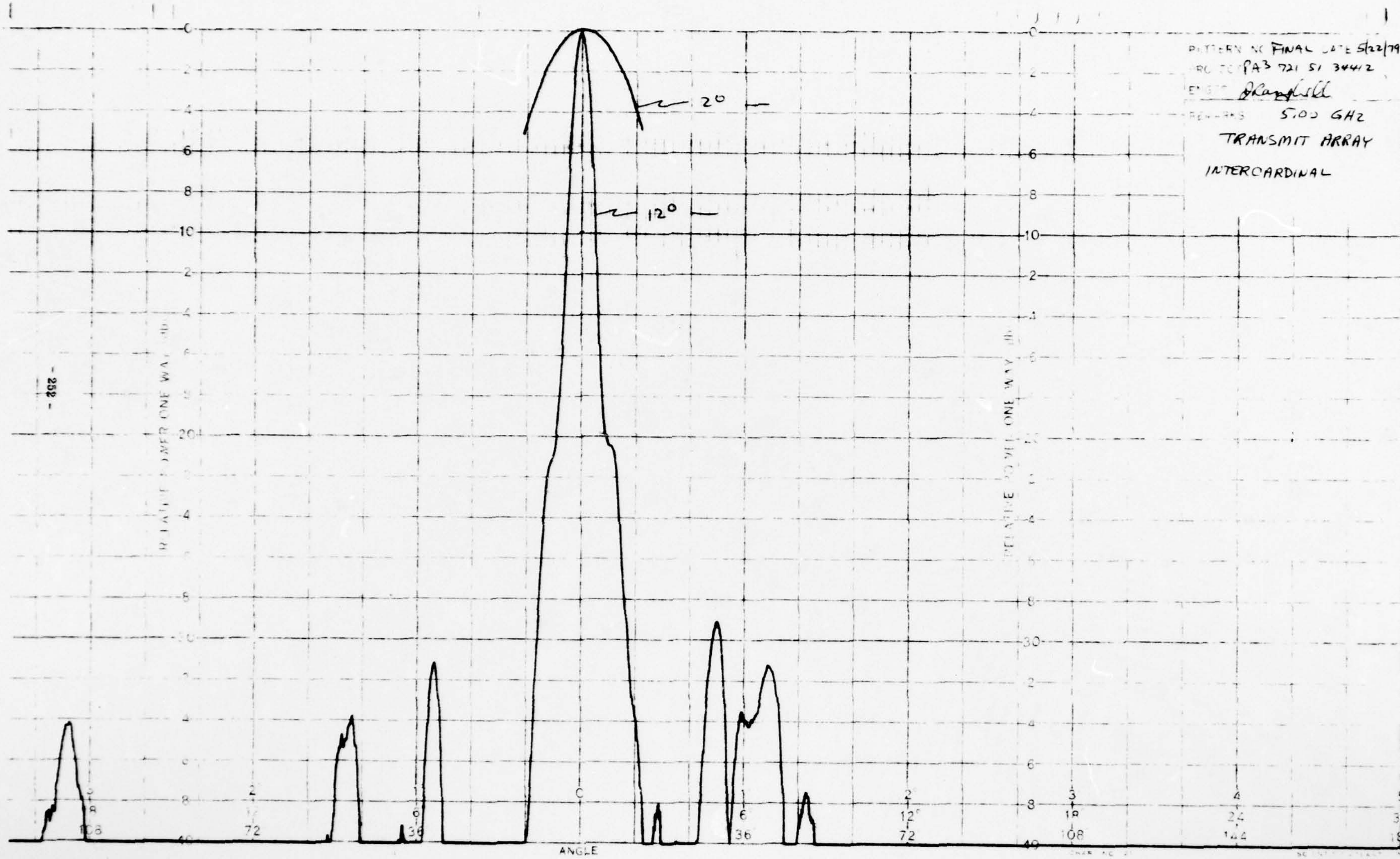
FINAL 5/22/79
PA3 721 51 344H?
4.4 GHz
TRANSMIT ARRAY
INTERCARDINAL
2°/DIV
12°/DIV
AZ
ANGLE

248 a


PATTERN NO FINAL DATE 5/26/78
PROJECT PA³ 721 57 34412
ENGRS
REMARKS 4.55 GHz
TRANSMIT ARRAY
INTERCARDINAL
RELATIVE POWER ONE WAY (db)
ANGLE
2°
12°

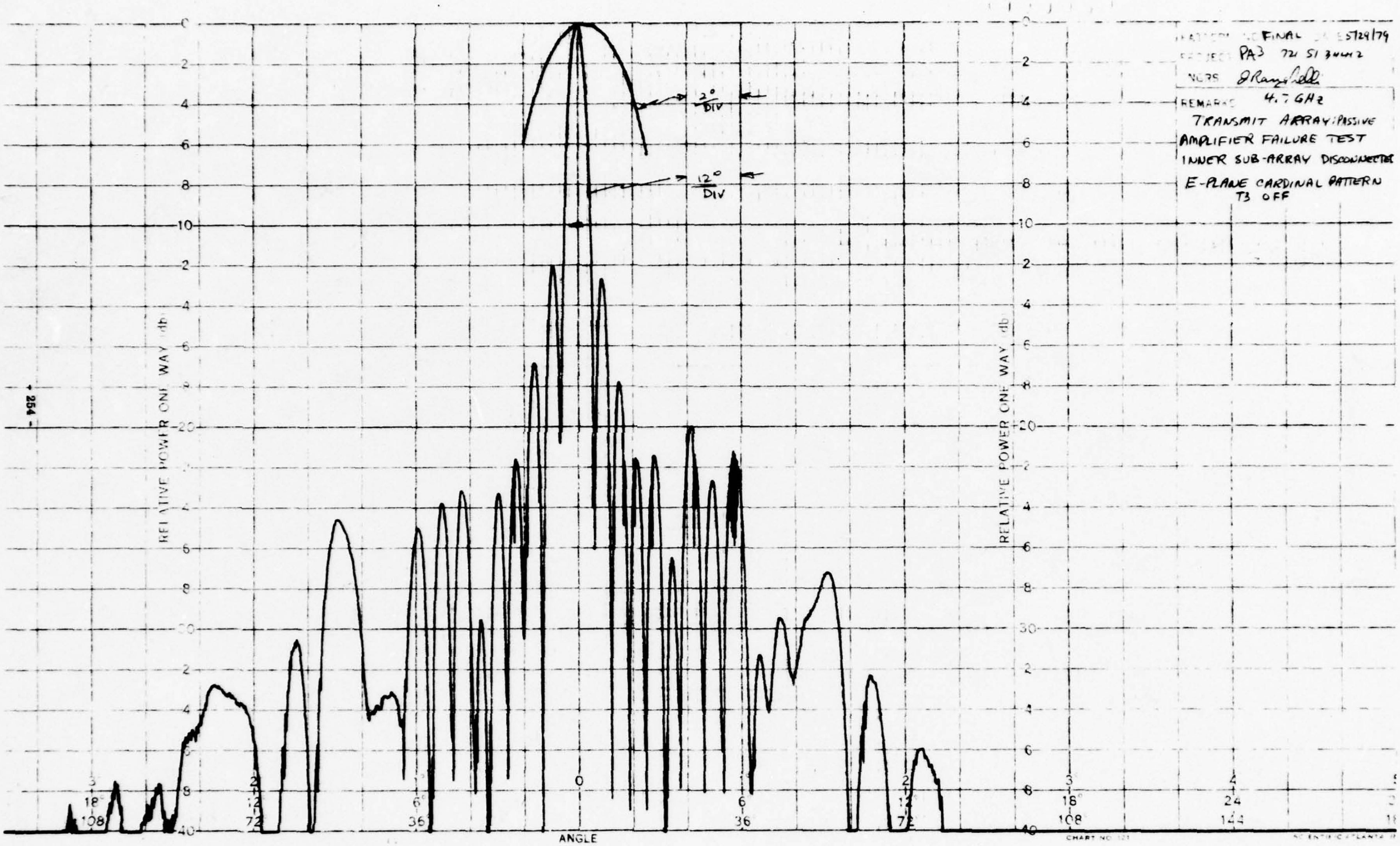

FINAL 5/22/79
PA³ 721 51 3441?
4.70 GHz
TRANSMIT ARRAY
INTERCARDINAL
2°
12°
RELATIVE POWER ONE WAY (db)
ANGLE

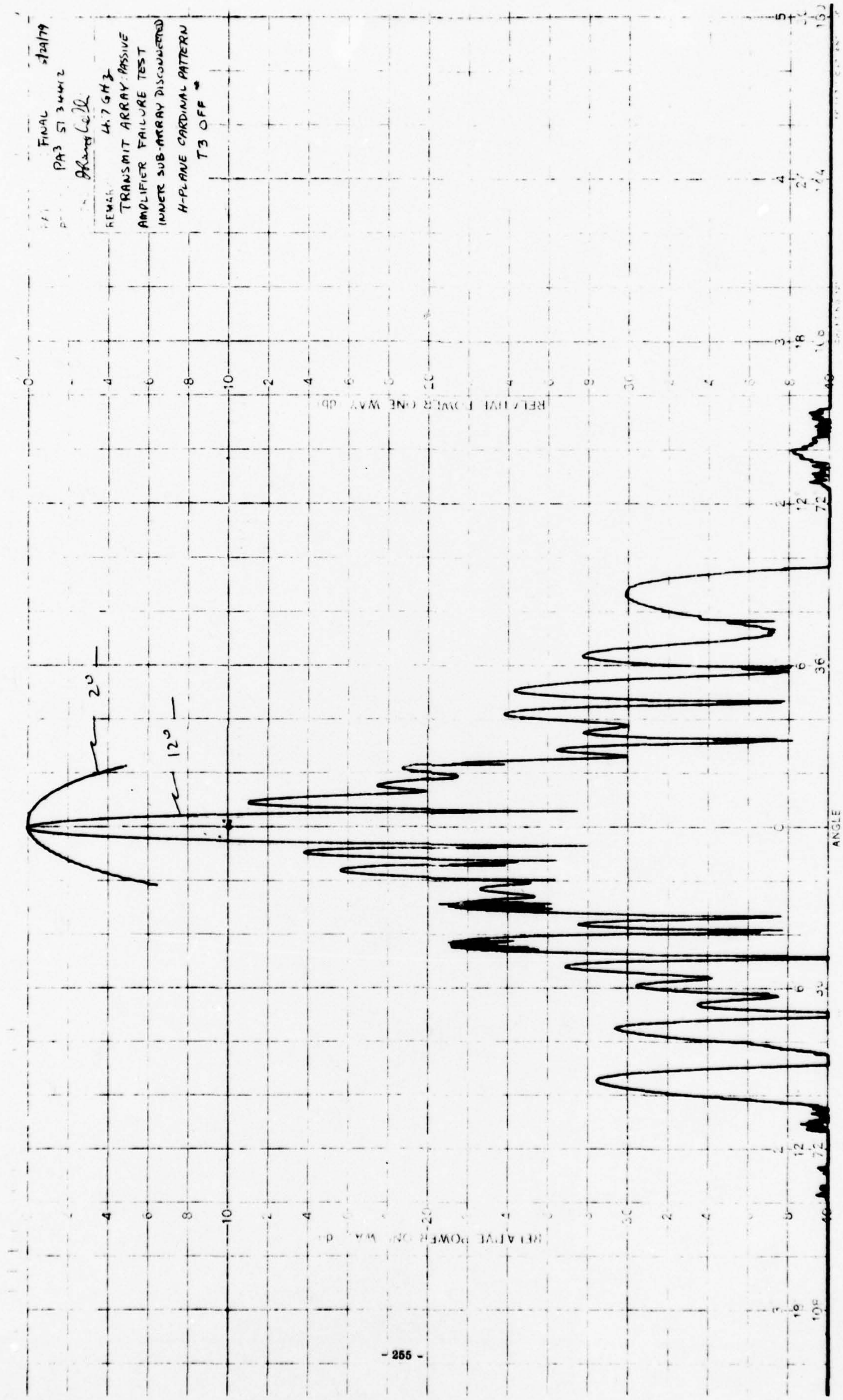

TRANSMIT ARRAY
INTERCARDINAL
4.85 GHz
2°
12°
ANGLE
RELATIVE POWER ONE WAY (dB)

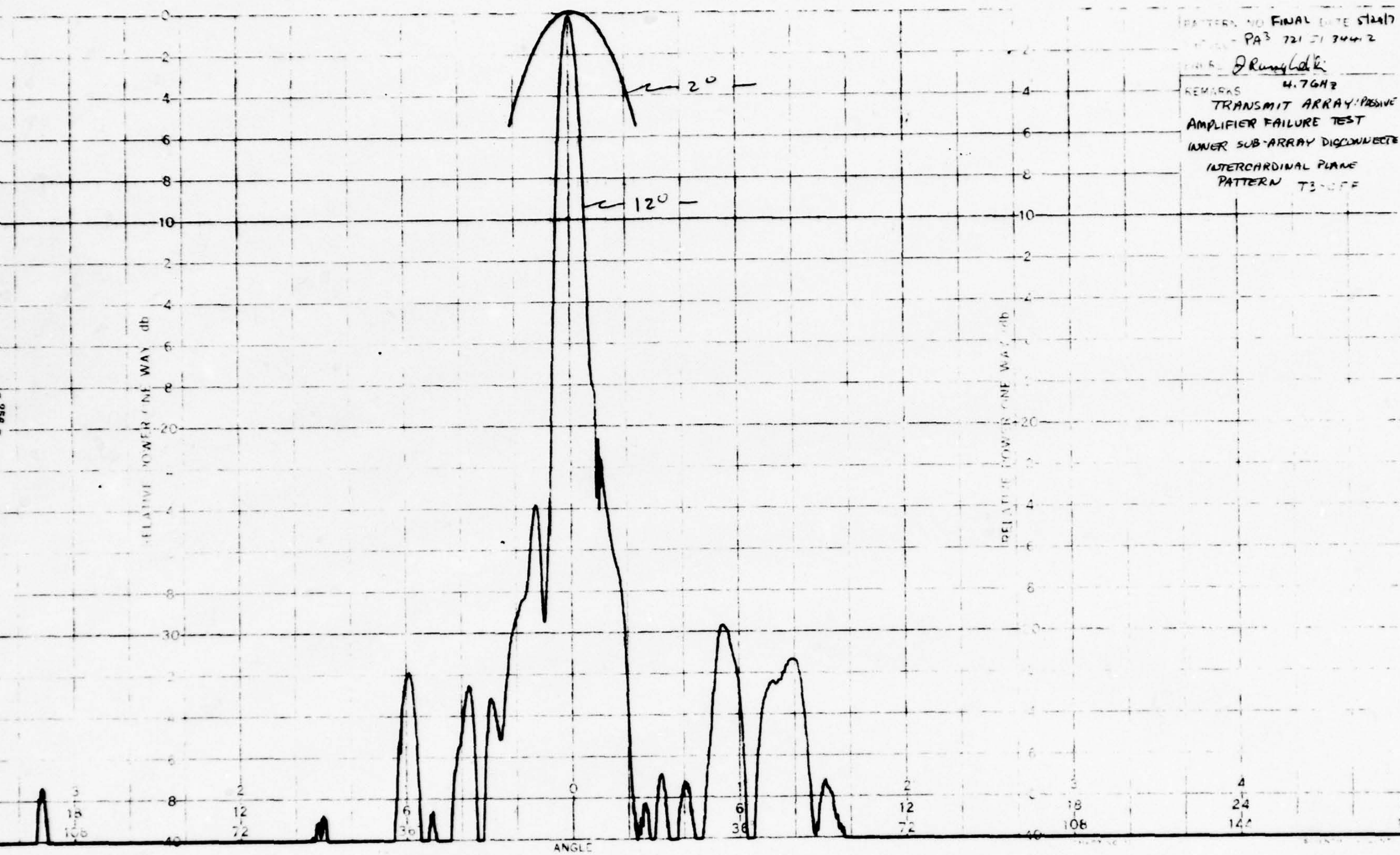


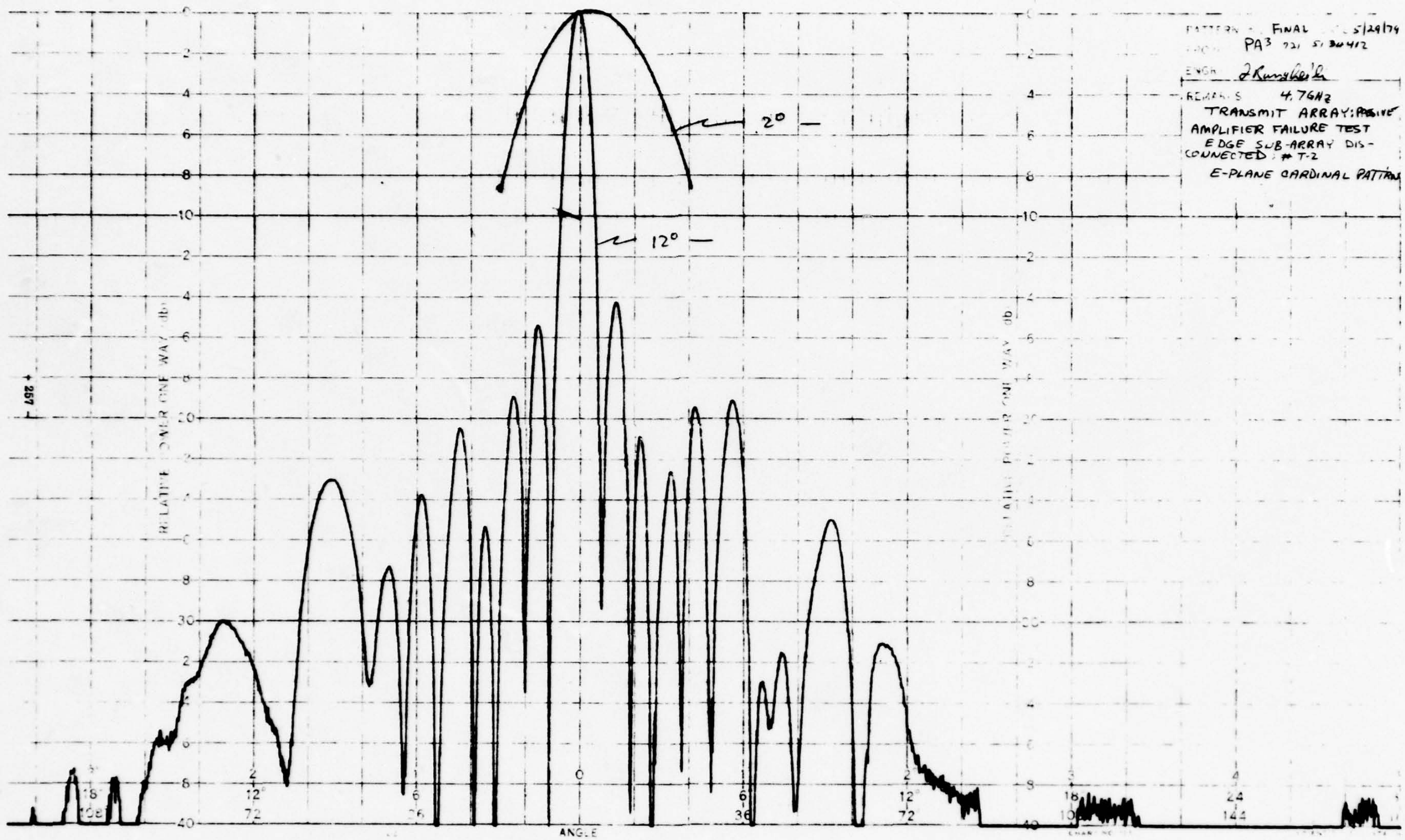
PATTERN NO FINAL DATE 5/22/79
PROJECT PA3 721 51 34412
ENGR. [signature]
REMARKS 5.00 GHz
TRANSMIT ARRAY
INTERCARDINAL
20
12°
RELATIVE POWER ONE WAY (dB)
ANGLE

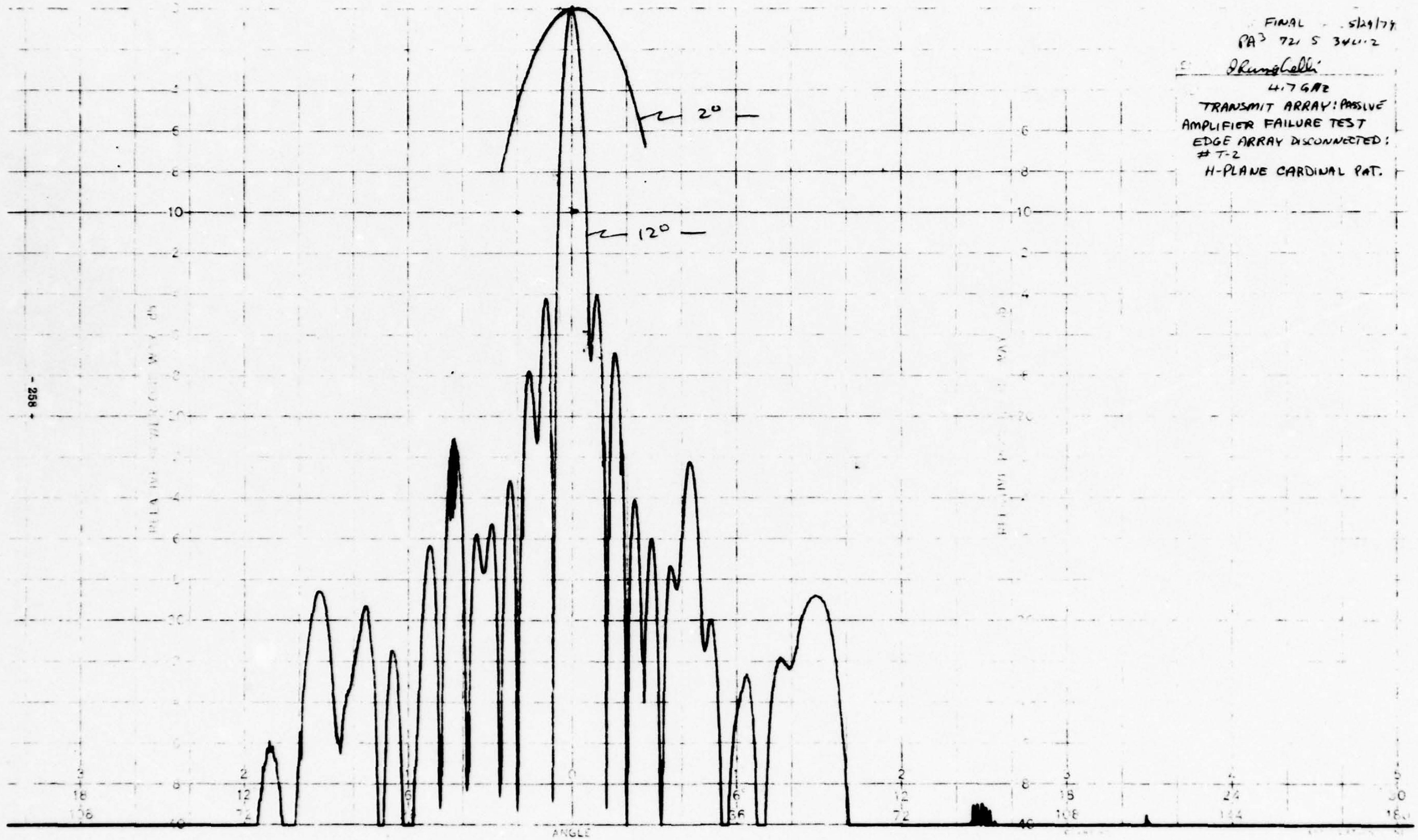
ANTENNA PATTERNS RESULTING FROM BPM
(SIMULATED) FAILURES

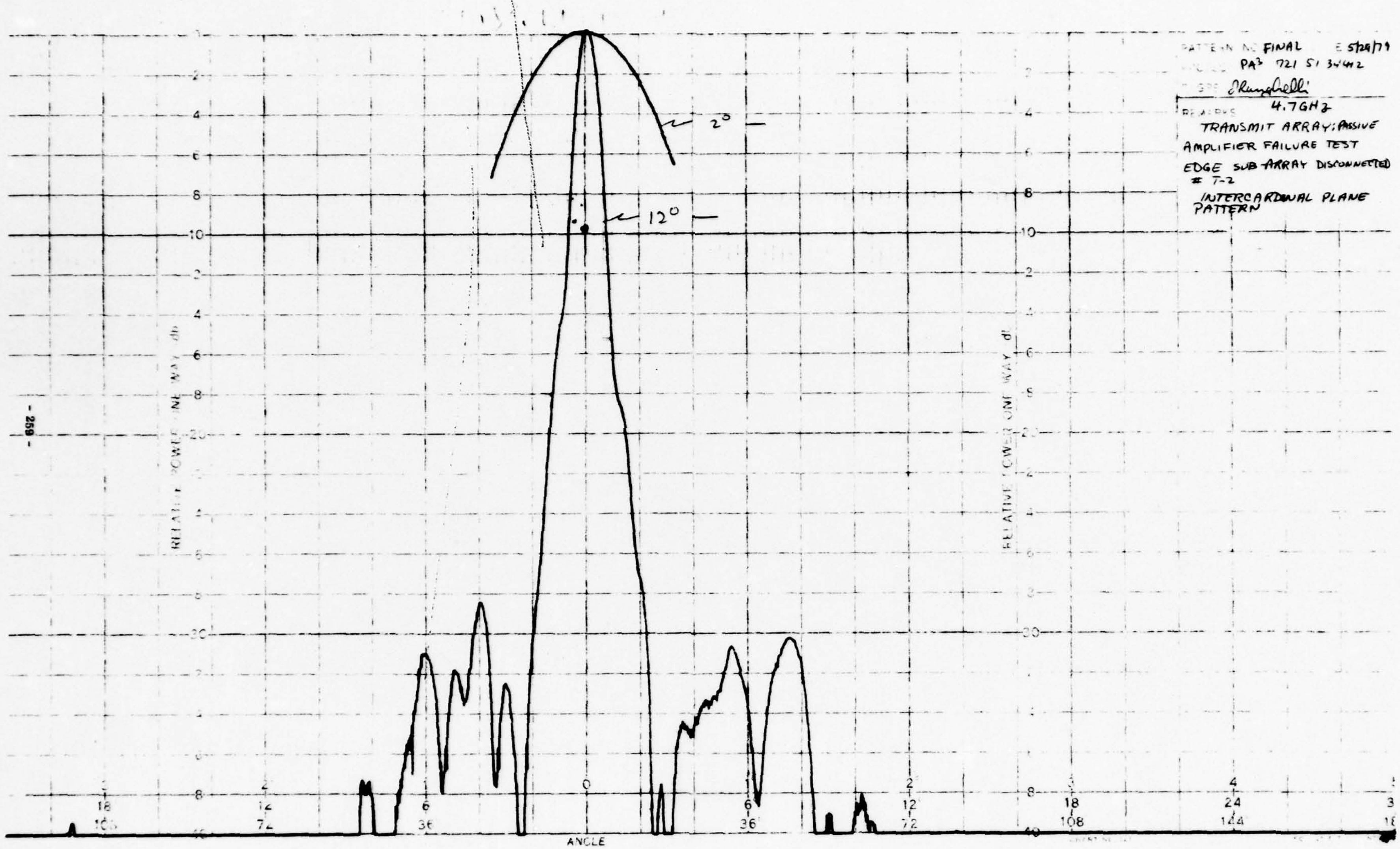

PATTERN NO FINAL DATE 5/24/79
PROJECT PA3 721 51 3 4.7 GHz
NOTES
REMARKS 4.7 GHz
TRANSMIT ARRAY: PASSIVE
AMPLIFIER FAILURE TEST
INNER SUB-ARRAY DISCONNECTED
E-PLANE CARDINAL PATTERN
T3 OFF
2°/DIV
12°/DIV
RELATIVE POWER ONE WAY (db)
ANGLE
CHART NO. 121


FINAL
PA3 ST 3 4412
REMARKS 4.7 GHz
TRANSMIT ARRAY · PASSIVE
AMPLIFIER FAILURE TEST
INNER SUB-ARRAY DISCONNECTED
H-PLANE CARDINAL PATTERN
T3 OFF
2°
12°
RELATIVE POWER ONE WAY (db)
ANGLE

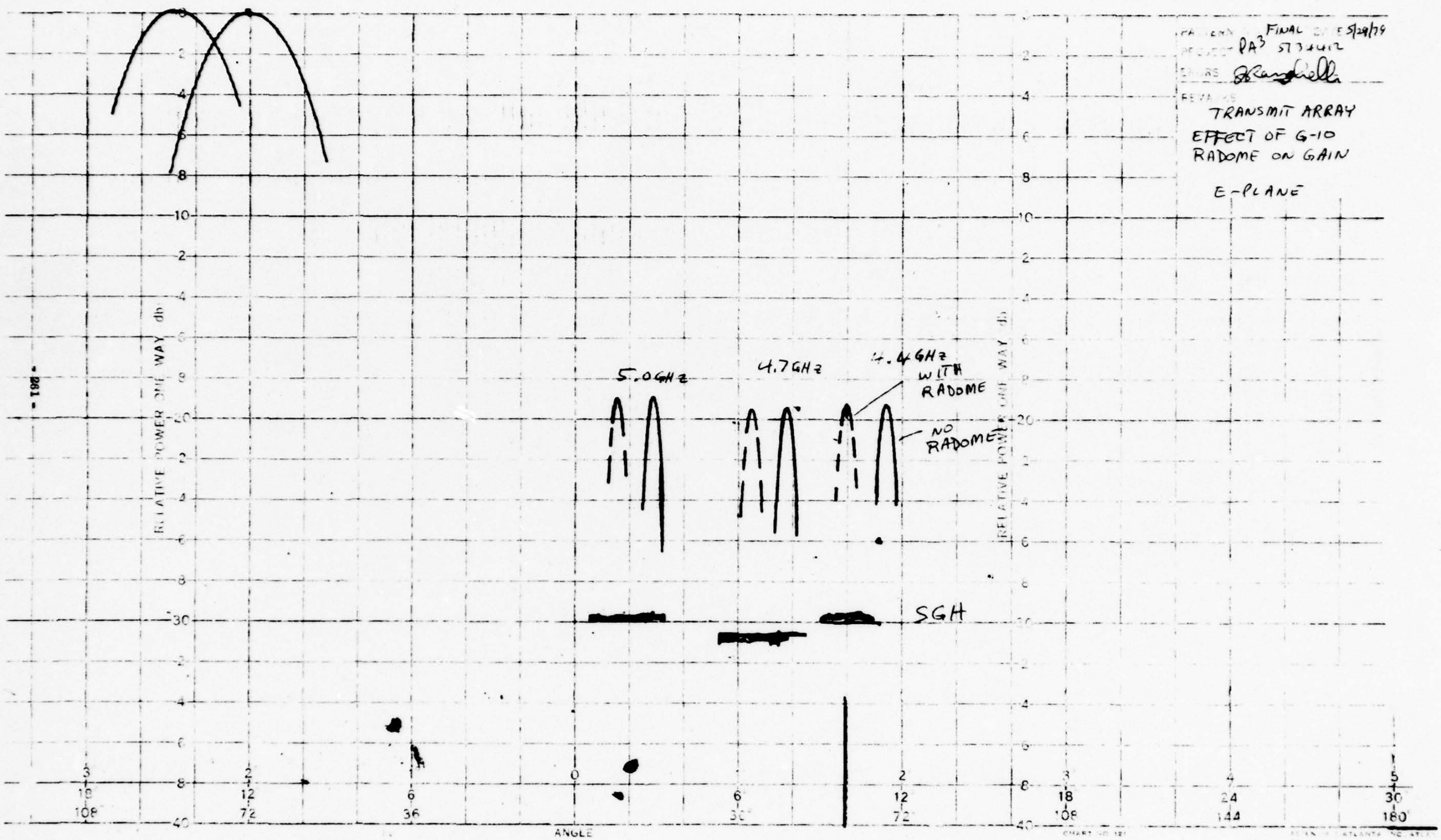

PATTERN NO FINAL DATE 5/24/7
PA3 721 51 344-2
4.7GHz
REMARKS
TRANSMIT ARRAY: PASSIVE
AMPLIFIER FAILURE TEST
INNER SUB-ARRAY DISCONNECTE
INTERCARDINAL PLANE
PATTERN T3-OFF
2°
12°
RELATIVE POWER ONE WAY db
ANGLE

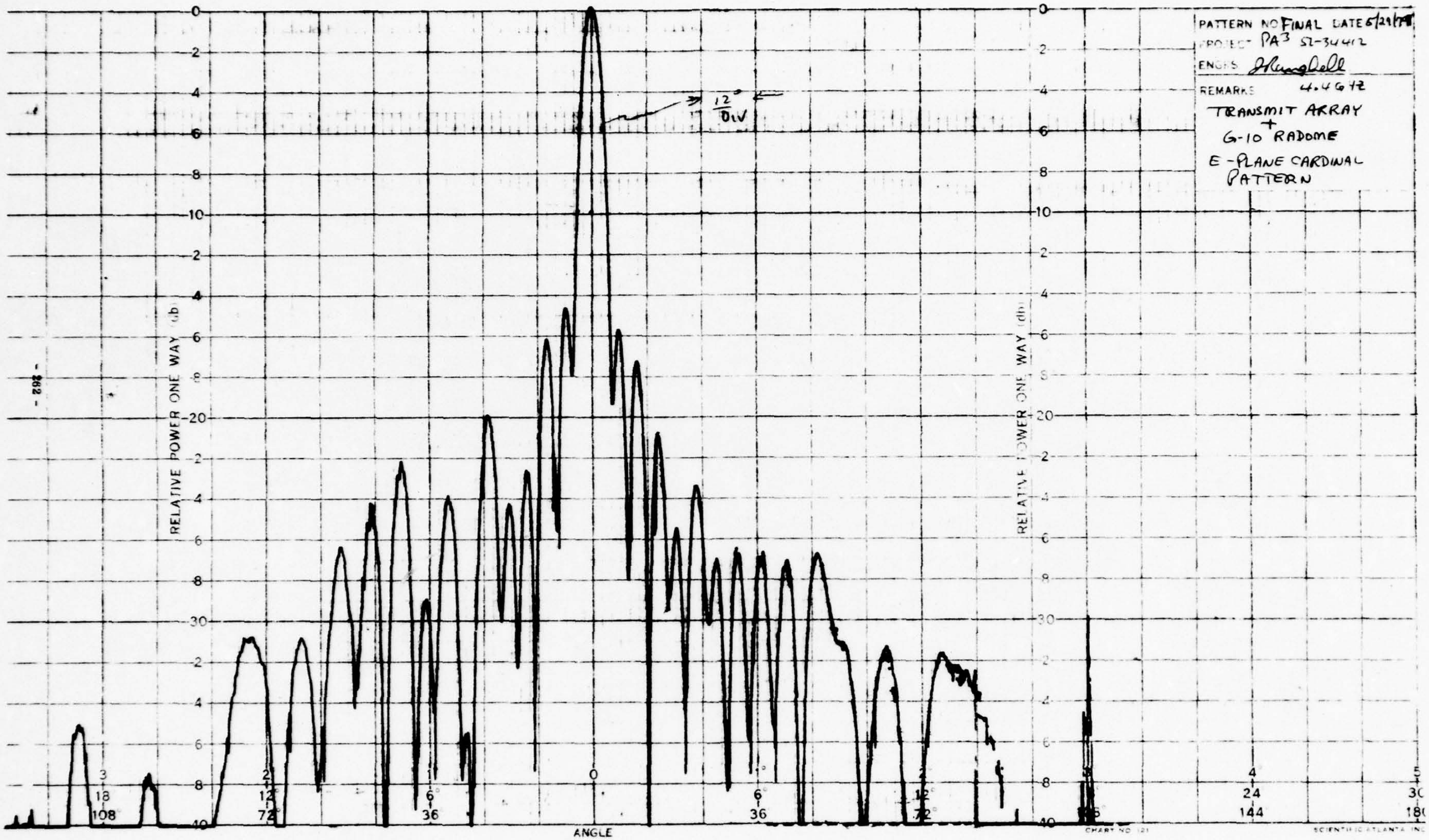

PATTERN FINAL 5/29/79
PA3 721 51 34412
ENGR
REMARKS 4.7GHz
TRANSMIT ARRAY: PASSIVE
AMPLIFIER FAILURE TEST
EDGE SUB-ARRAY DIS-
CONNECTED; # T-2
E-PLANE CARDINAL PATTERN
2°
12°
RELATIVE POWER ONE WAY db
ANGLE

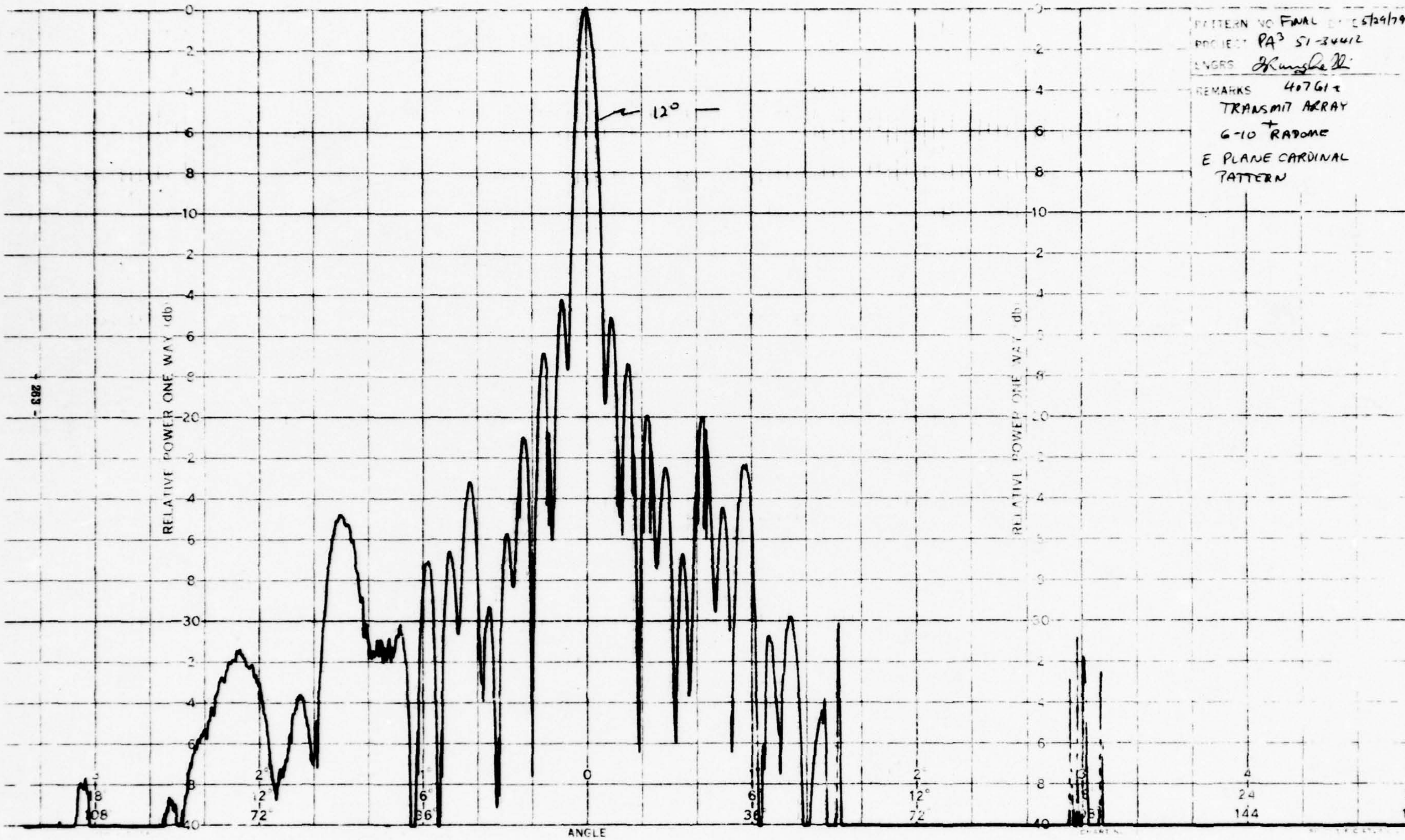

FINAL 5/29/77
4.7 GHz
TRANSMIT ARRAY: PASSIVE
AMPLIFIER FAILURE TEST
EDGE ARRAY DISCONNECTED:
T-2
H-PLANE CARDINAL PAT.
2°
12°
ANGLE

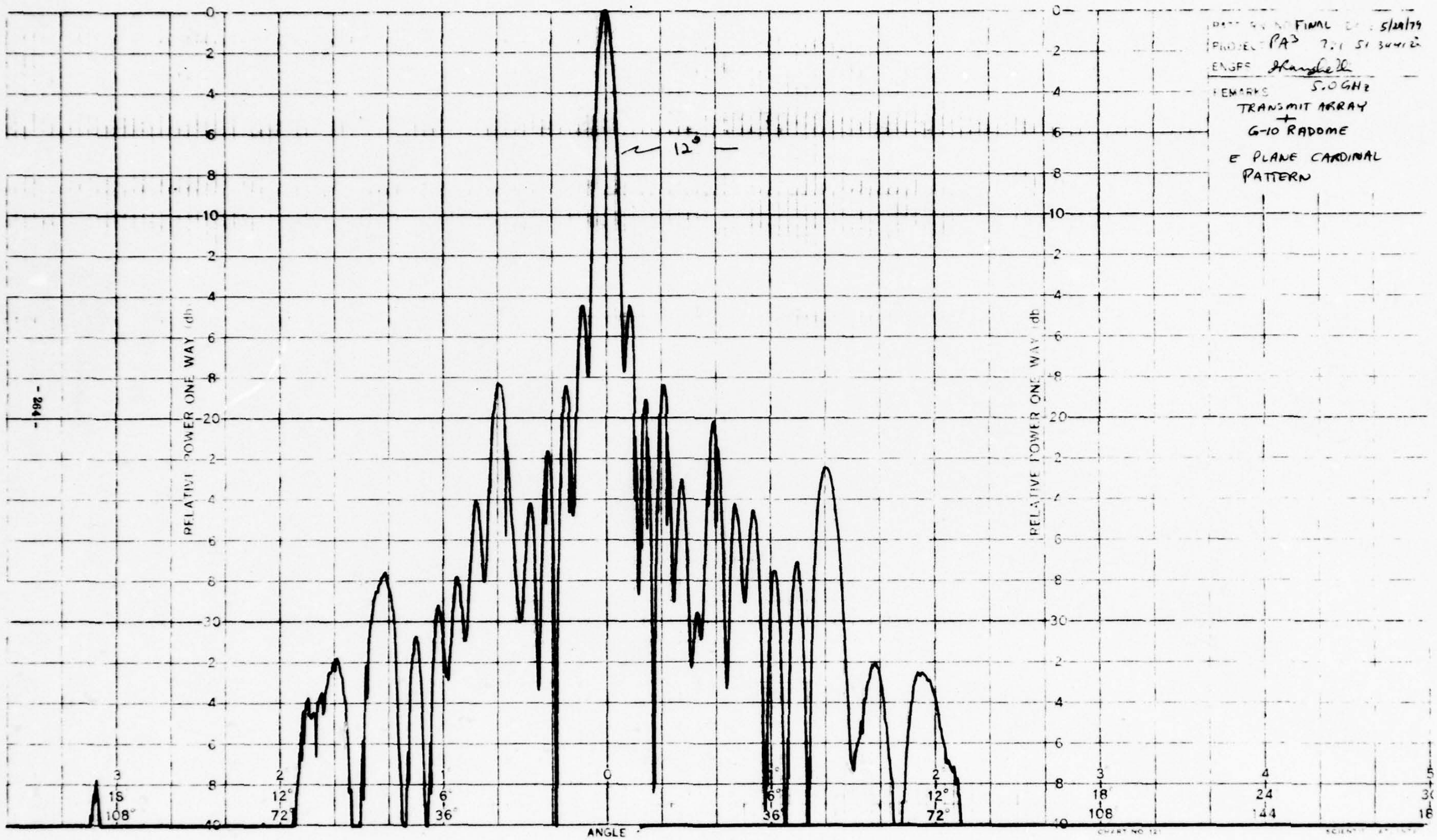

PATTERN NO FINAL
E 5/24/79
PA3 721 51 34412
4.7GHz
TRANSMIT ARRAY; PASSIVE
AMPLIFIER FAILURE TEST
EDGE SUB ARRAY DISCONNECTED
7-2
INTERCARDINAL PLANE
PATTERN
2°
12°
RELATIVE POWER ONE WAY db
ANGLE

ANTENNA PATTERNS AND GAIN RESULTING FROM
USE OF G 10 EPOXY FIBER GLASS RADOME


FINAL DATE 5/29/79
PA3 573412
TRANSMIT ARRAY
EFFECT OF G-10
RADOME ON GAIN
E-PLANE
5.0GHz
4.7GHz
4.4GHz
WITH
RADOME
NO
RADOME
SGH
RELATIVE POWER ONE WAY db
ANGLE


PATTERN NO FINAL DATE 5/29/78
PROJECT PA3 52-34412
ENGRS. [illegible signature]
REMARKS 4.4 GHz
TRANSMIT ARRAY + G-10 RADOME
E-PLANE CARDINAL PATTERN
12°/DIV
RELATIVE POWER ONE WAY (db)
ANGLE
CHART NO 121
SCIENTIFIC ATLANTA INC


PATTERN NO FINAL DATE 5/29/79
PROJECT PA³ 51-34412
ENGRS
REMARKS 40761 TRANSMIT ARRAY + 6-10 RADOME
E PLANE CARDINAL PATTERN
12°
RELATIVE POWER ONE WAY (db)
ANGLE



FINAL 5/29/79
PROJECT PA³
ENGRS
REMARKS 5.0 GHz
TRANSMIT ARRAY
+
G-10 RADOME
E PLANE CARDINAL
PATTERN
12°
RELATIVE POWER ONE WAY (db)
ANGLE

B EXTENDED AMPLIFIER TESTS

1. Gallium Arsenide FET

As part of the high power amplifier technology investigation, several additional test, not required by contract, were performed.

Following is a listing of these test:

1) AM/PM Conversion
2) 2 Tone 3rd Order Intercept Point
3) Noise Power
4) Turn on Characteristics
5) Efficiency Versus Drive

The data from these tests follows.

IPA DATA

I] Pout & Eff versus Pin

V_{DS} = 8.5V I_{TOT} (NO DRIVE) = 1.0 amp

	4.4 ghz		4.7 ghz		5.0 ghz	
Pin	Pout	Itot	Pout	Itot	Pout	Itot
+ 10 dBm	-6.5 dBm	.97a	-6.0	1.0 a	-5.9	.97a
+ 15 dBm	-.6	.97	-1.0	1.0	-0.9	.97a
+ 16 dBm	+.3	.97	0	1.0	+0.1	.97
+ 17 dBm	+1.2	.97	+.9	1.01	+1.0	.98
+ 18 dBm	+2.0	.98	+1.75	1.03	+1.7	.98
+ 19 dBm	+2.65	1.0	+2.6	1.06	+2.5	.99
+ 20 dBm	+3.1	1.03	+3.3	1.1	+2.9	1.0

CALIB 29.5 dB at 4.4 Ghz
29.6 dB at 4.1 Ghz
29.6 dB at 5.0 Ghz

II DETECTOR VOLTAGE

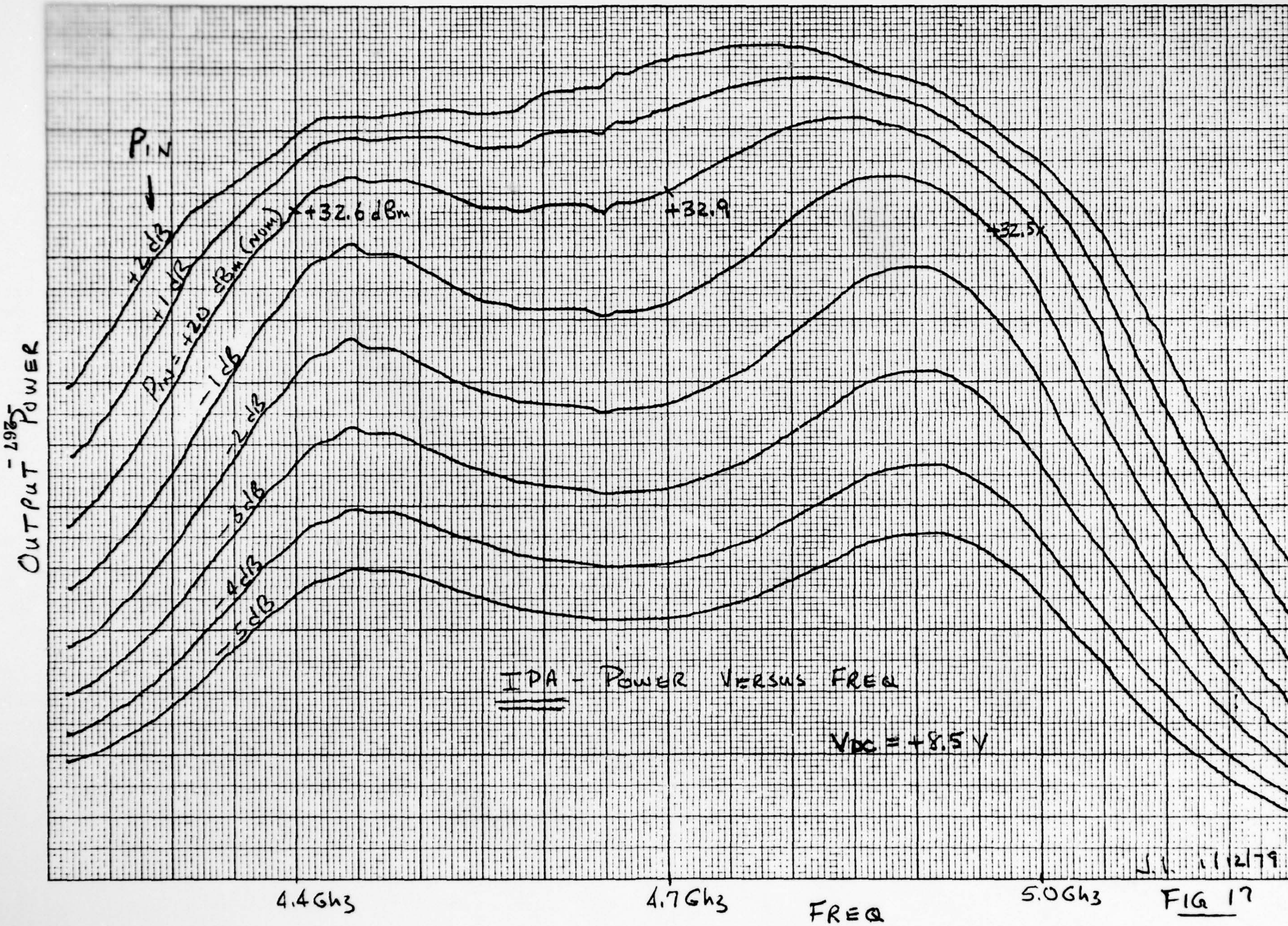
	VDET		
Pout	4.4 ghz	4.7 ghz	5.0 ghz
+33 dBm	-1.68 v	-1.66 v	-1.67 v
+32	-1.40 v	-1.47 v	-1.48 v
+31	-1.18 v	-1.29 v	-1.33 v
+30	-0.99 v	-1.12 v	-1.17 v

TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION 2 PLACE	3 PLACE	ANGLES	IPA DATA
USED ON		CODE IDENT. NO. 28528	DWG. SIZE A	PHASED ARRAY
PREPARED BY DATE				
CHECKED BY DATE				SHEET

DRAWING NUM

ITT DEFENSE COMMUNICATIONS DIVISION NUTLEY, NEW JERSEY

D5216 A REV. 5/73


PIN
+2 dB
+1 dB
PIN = +20 dBm (NOM)
+32.6 dBm
+32.9
+32.5
-1 dB
-2 dB
-3 dB
-4 dB
-5 dB
IPA - POWER VERSUS FREQ
VDC = +8.5 V
OUTPUT POWER
4.4 Ghz
4.7 Ghz
5.0 Ghz
FREQ
J.I. 1/12/79
FIG 17

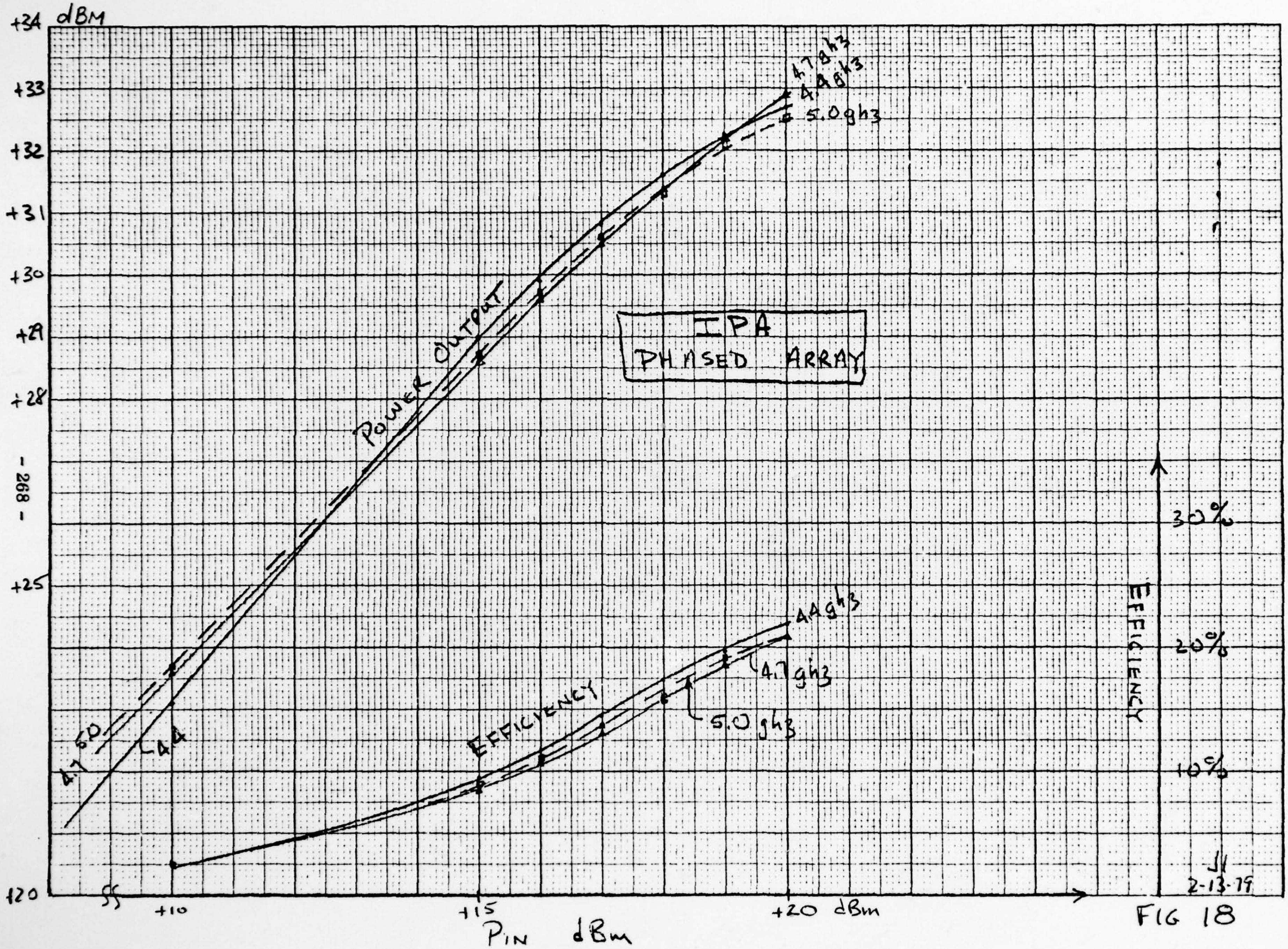
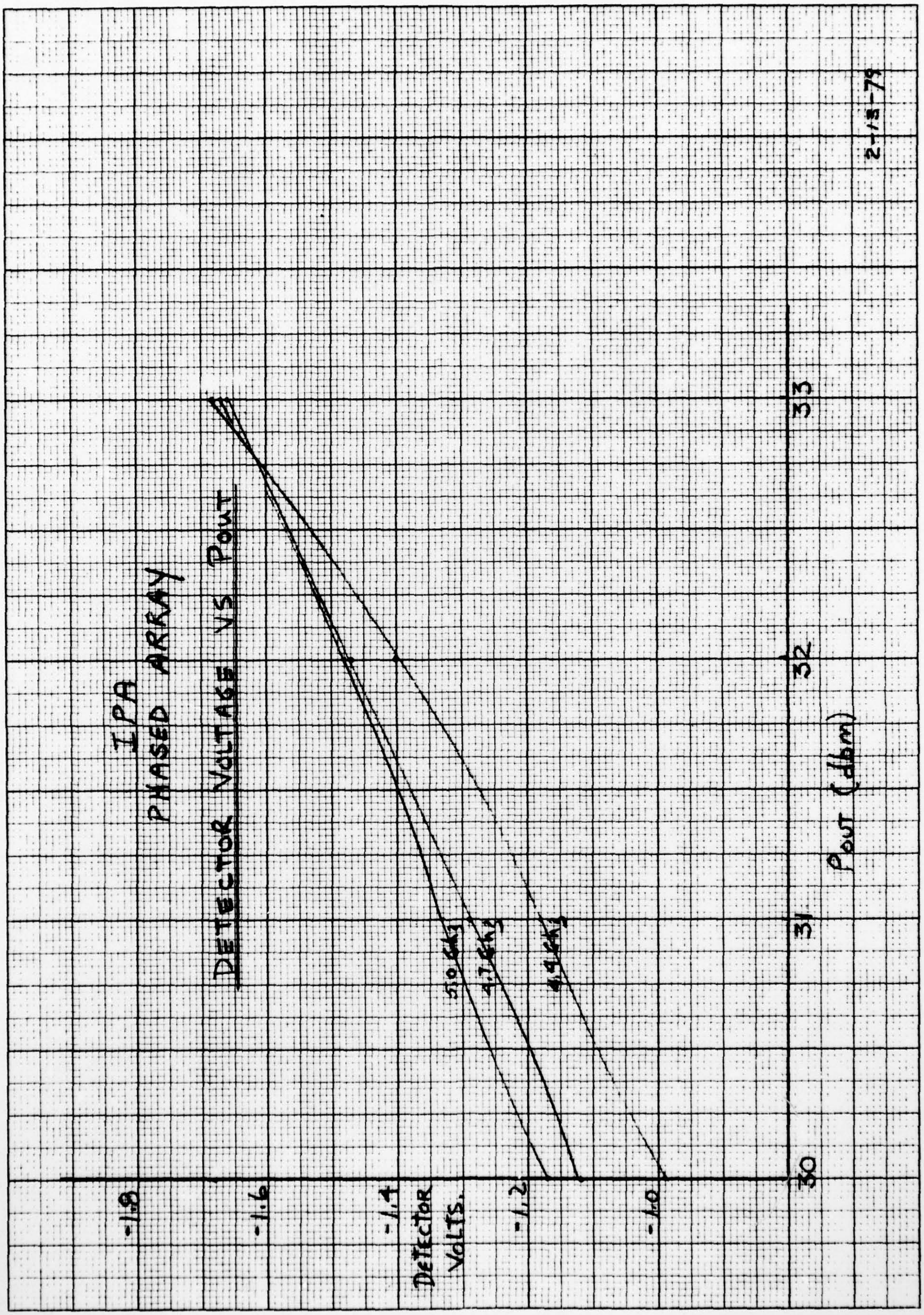
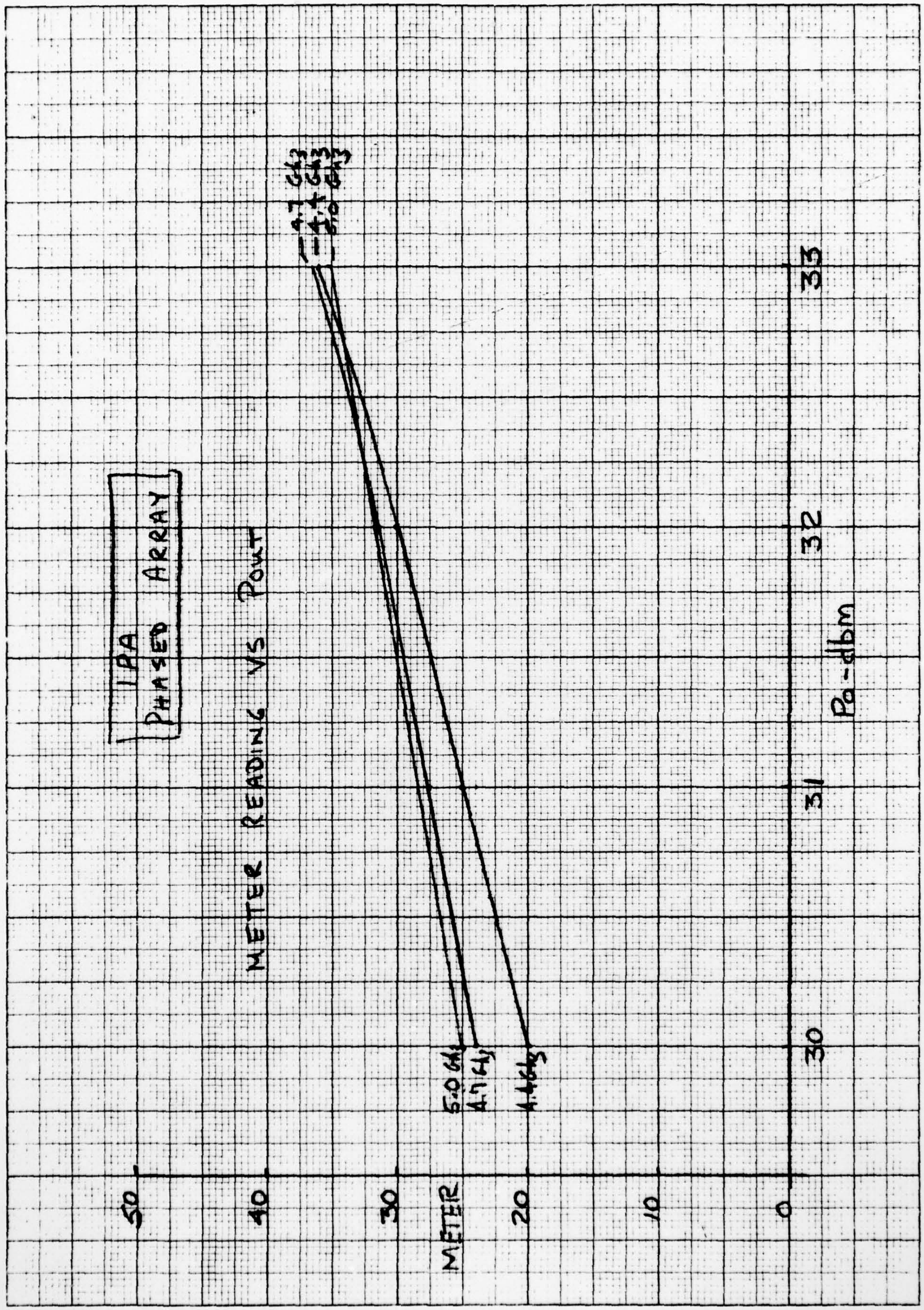

+34 dBM
+33
+32
+31
+30
+29
+28
+25
+20
+10
+15
+20 dBm
PIN dBm
POWER OUTPUT
IPA
PHASED ARRAY
4.7 ghz
4.4 ghz
5.0 ghz
4.7
5.0
4.4
EFFICIENCY
4.4 ghz
4.7 ghz
5.0 ghz
30%
20%
10%
EFFICIENCY
JT
2-13-79

FIG 18


IPA
PHASED ARRAY
DETECTOR VOLTAGE VS POUT
-1.8
-1.6
-1.4
-1.2
-1.0
Detector
Volts.
30
31
32
33
POUT (dbm)
5.0 GHz
4.7 GHz
4.4 GHz
2-13-79


IPA
PHASED ARRAY
METER READING VS POUT
Po-dbm
METER
50
40
30
20
10
0
30
31
32
33
5.0 GHz
4.7 GHz
4.4 GHz

BPM - SER # 1

I] POUT VERSUS PIN / EFFICIENCY VERSUS PIN

PIN	4.4 Ghz Po	4.4 Ghz ITOT	4.7 Ghz Po	4.7 Ghz ITOT	5.0 Ghz Po	5.0 Ghz ITOT
~~+10~~						
+15	-2.55 dBm	1.56a	-2.0 dBm	1.55a	-3.5 dBm	1.52a
~~+18~~						
+20	+2.8	1.72	+2.30	1.70	+1.05	1.60
+21	+3.5	1.80	+3.60	1.85	+1.45	1.62
+22	+4.05	1.90	+4.85	2.02	+2.0	1.65
+23	+5.1	2.08	+5.85	2.20	+3.0	1.75
+24	+6.2	2.32	+6.4	2.35	+4.0	1.89
+25	+6.5	2.40	+6.6	2.42	+4.85	2.03
+25.4	+6.55	2.42	+6.6	2.43	+5.1	2.08

VDS = 8.5v

CALIB = 29.5dB at 4.4Ghz, 29.6 dB at 4.7, 29.6dB at 5.0Ghz

II] DETECTOR VOLTAGE

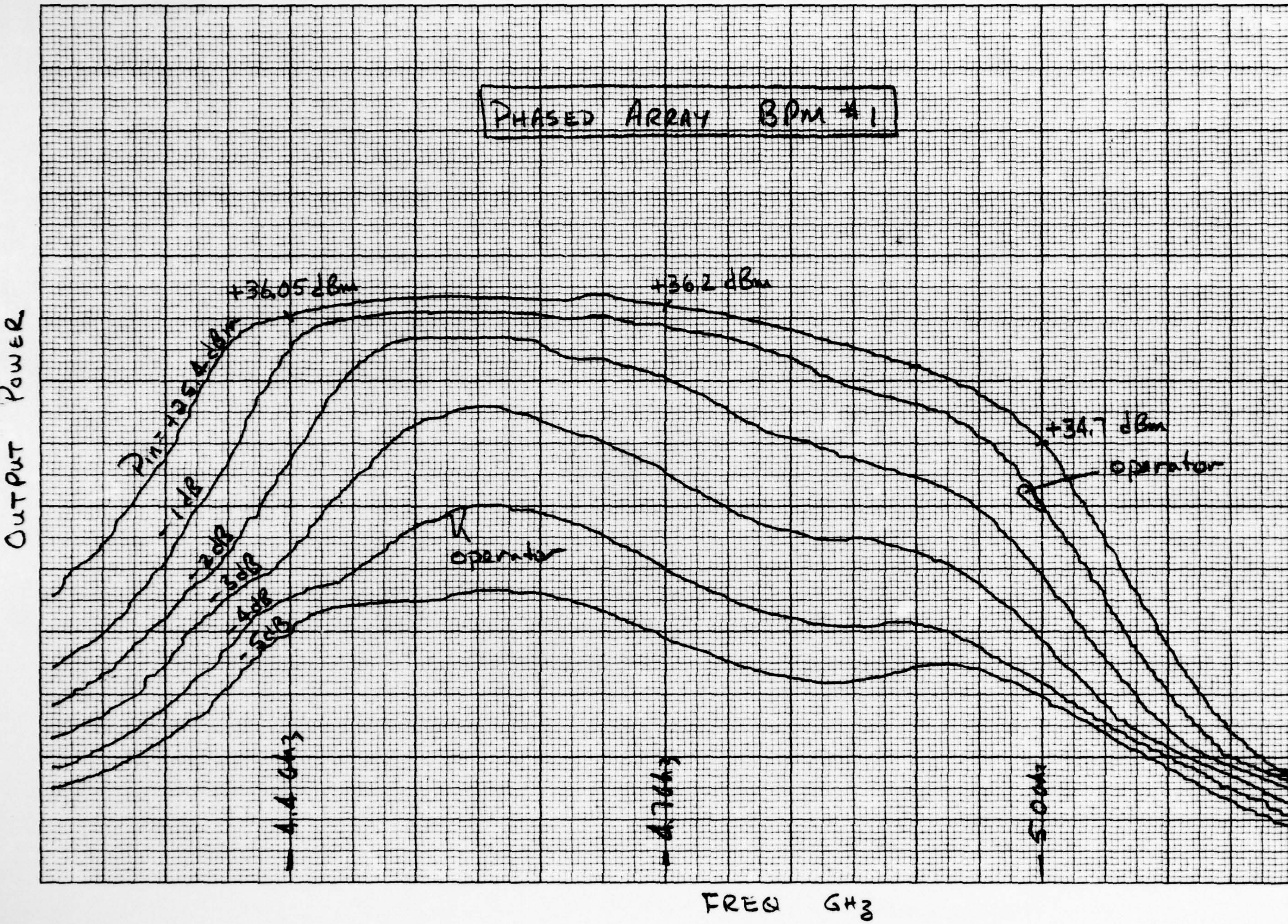
POUT	VDET 4.4	4.7	5.0
+36 dBm	-.86 volt	-1.34	—
+35 dBm	-.71	-1.02	-.83
+33 dBm	-.52	-.73	-.60
+30 dBm	-.28	-.46	-.35

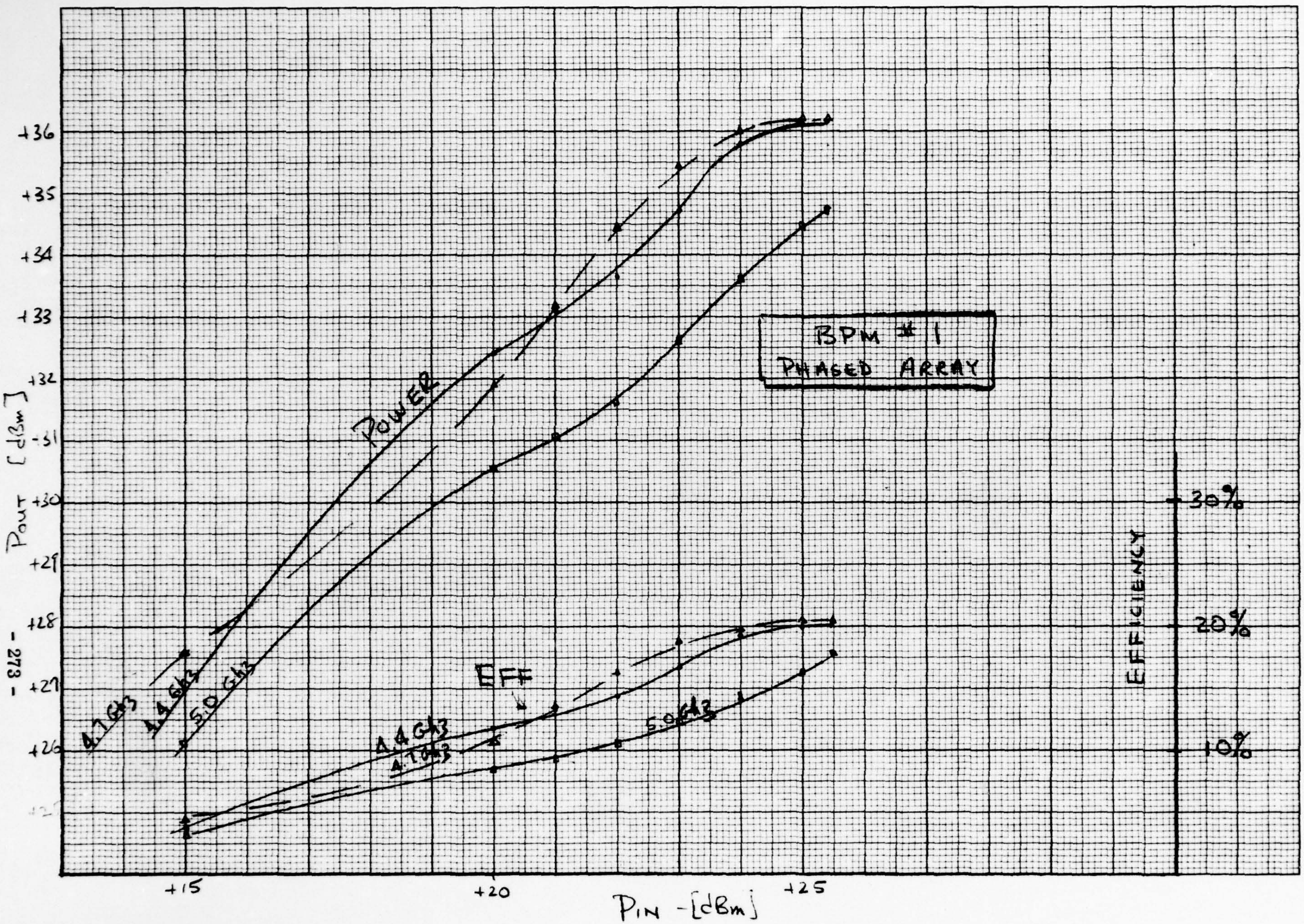
DRAWING NUMBER

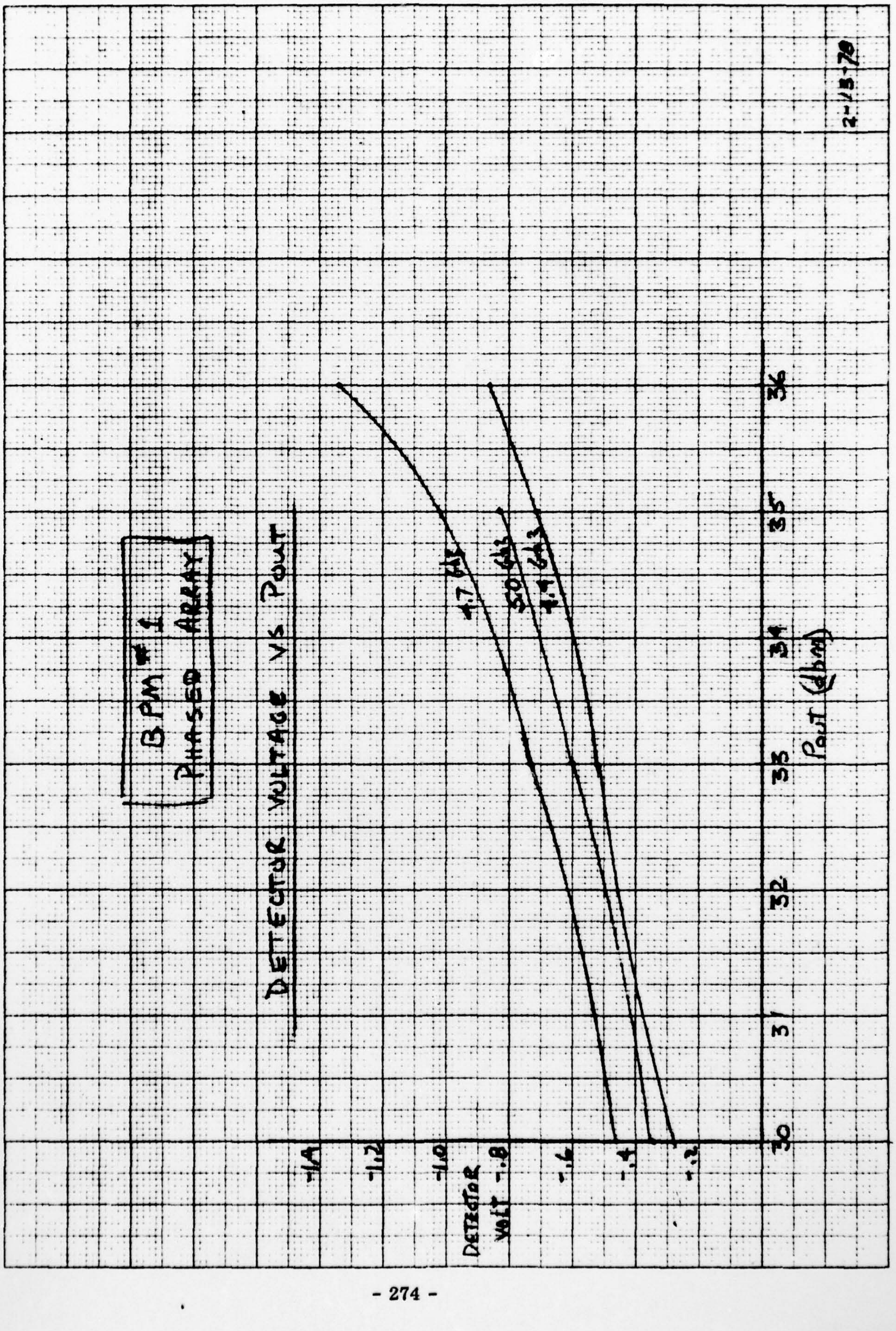
ITT DEFENSE COMMUNICATIONS DIVISION NUTLEY, NEW JERSEY

TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION 2 PLACE	3 PLACE	ANGLES	PHASED ARRAY AMPL's
USED ON	CODE IDENT. NO. 28528	DWG. SIZE A		
PREPARED BY / DATE				
CHECKED BY / DATE				SHEET

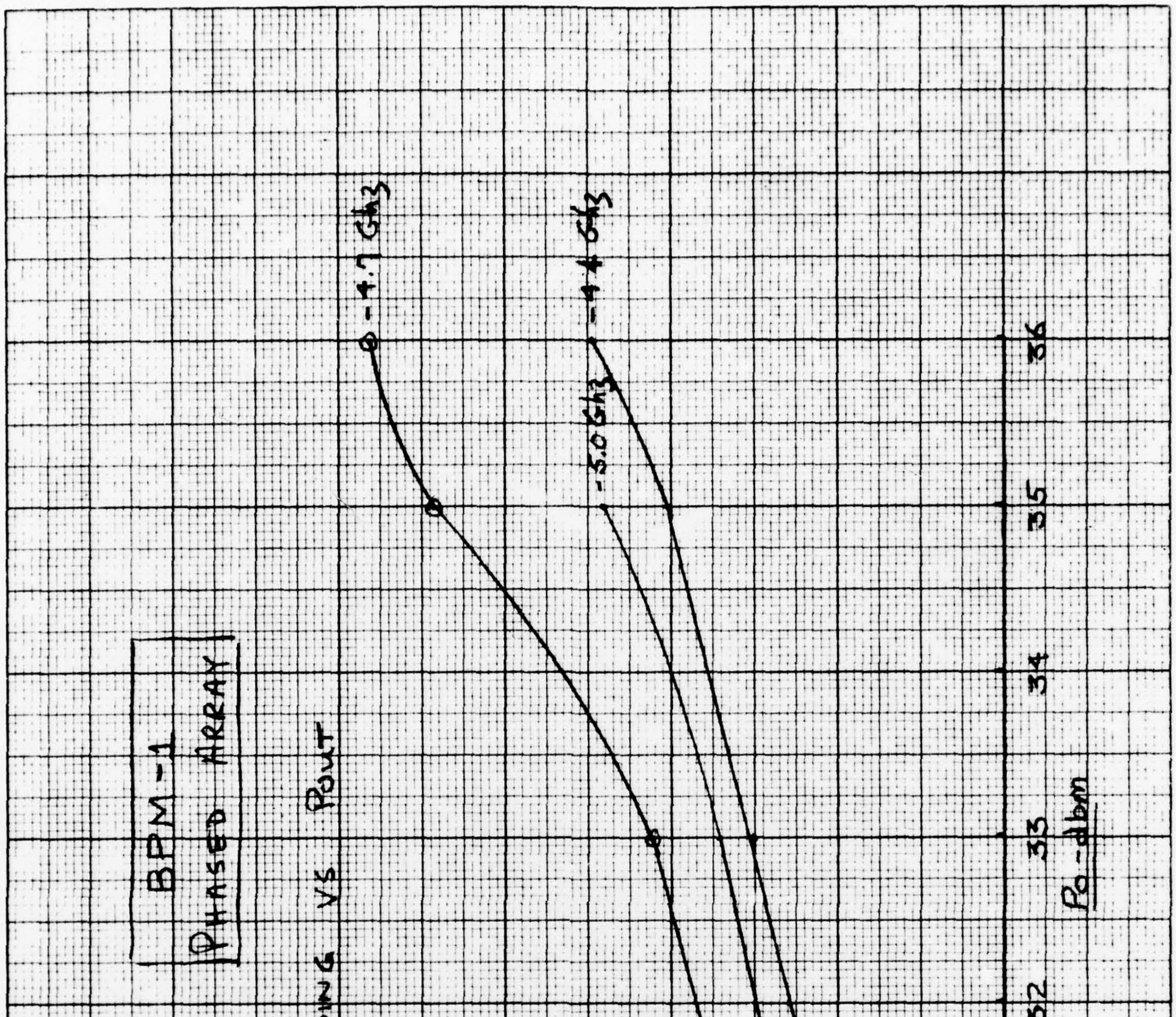
D5215 A REV. 5/73


PHASED ARRAY BPM #1
OUTPUT POWER
FREQ GHz
+36.05 dBm
+36.2 dBm
+34.7 dBm
Pin=+35.4 dBm
-1dB
-2dB
-3dB
-4dB
-5dB
operator
operator
4.4 GHz
4.7 GHz
5.0 GHz


BPM # 1
PHASED ARRAY
POWER
EFF
4.7 GHz
4.4 GHz
5.0 GHz
4.4 GHz
4.1 GHz
5.0 GHz
EFFICIENCY
30%
20%
10%
+36
+35
+34
+33
+32
+31
+30
+29
+28
+27
+26
POUT [dBm]
+15
+20
+25
PIN -[dBm]



BPM # 1
PHASED ARRAY
DETECTOR VOLTAGE VS POUT
4.7 GHz
5.0 GHz
4.4 GHz
-1.4
-1.2
-1.0
DETECTOR VOLT -.8
-.6
-.4
-.2
30
31
32
33
34
35
36
Pout (dbm)
2-13-78


BPM-1
PHASED ARRAY
METER READING VS POUT
-4.7 GHz
-4.4 GHz
-5.0 GHz
30
31
32
33
34
35
36
Po - dbm
METER (uA)
50
40
30
20
10
0

BPM - SER # 2

I] POUT VERSUS PIN / EFFICIENCY VERSUS PIN

PIN	4.4 Ghz Po	4.4 Ghz ITOT	4.7 Ghz Po	4.7 Ghz ITOT	5.0 Ghz Po	5.0 Ghz ITOT
~~+10~~						
+15	-1.6 dBm	2.12a	-0.4 dBm	2.10a	-1.15 dBm	2.10a
~~+18~~						
+20	+3.0	2.17	+3.3	2.10	+2.8	2.06
+21	+3.85	2.18	+4.0	2.05	+3.4	2.05
+22	+4.5	2.20	+4.5	2.0	+3.95	2.03
+23	+5.15	2.18	+5.2	1.92	+4.3	2.01
+24	+5.75	2.13	+5.8	1.90	+4.8	1.95
+25	+6.25	2.13	+6.25	1.92	+5.3	1.86
+25.4	+6.45	2.14	+6.35	1.93	+5.5	1.84

VDS = 8.5 V

CALIB = 29.5dB at 4.4Ghz, 29.6 dB at 4.7, 29.6 dB at 5.0 Ghz

II] DETECTOR VOLTAGE

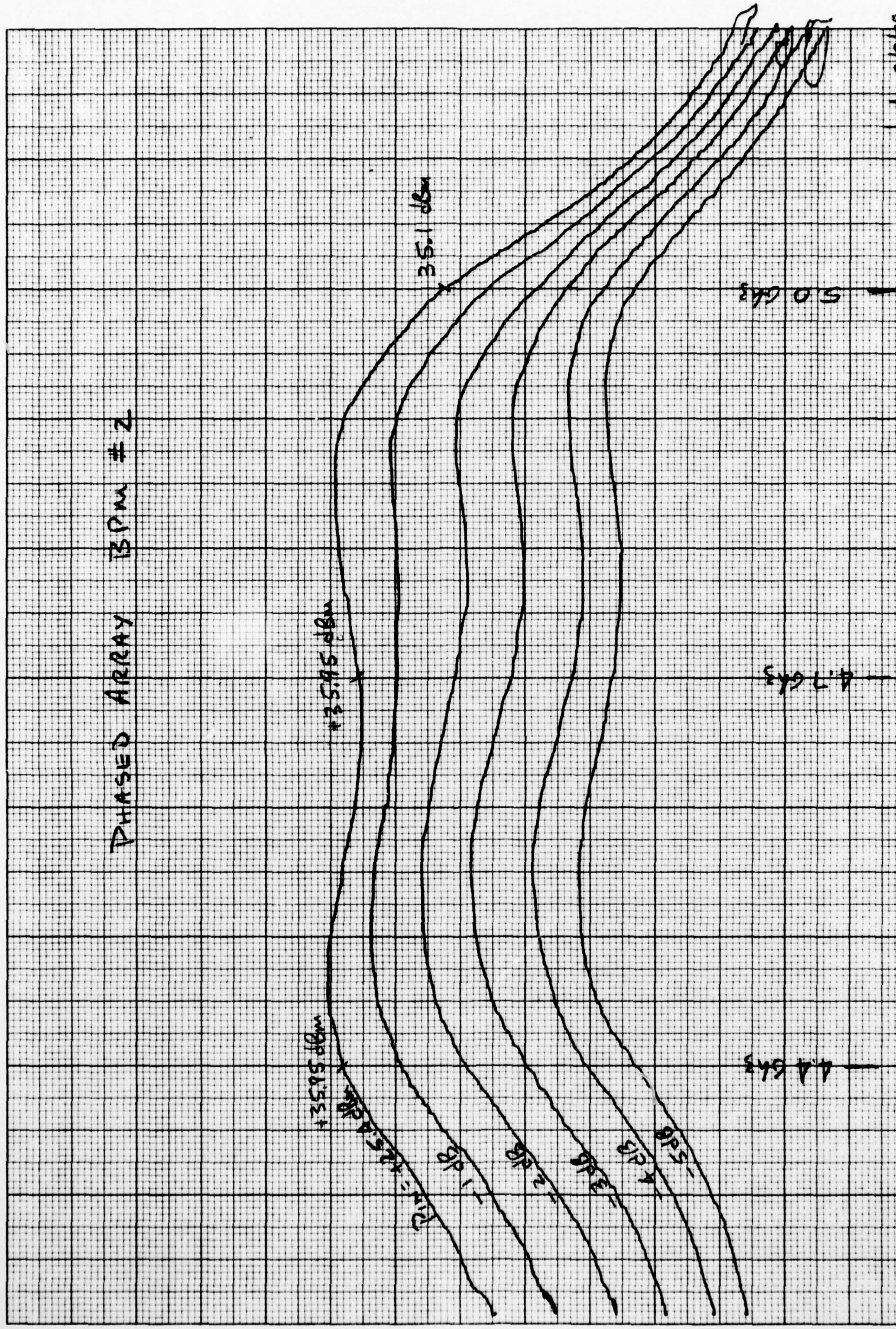
POUT	VDET 4.4	4.7	5.0
+36 dBm	-.51 v	-1.05 v	-.62 v
+35 dBm	-.45	-.92	-.51
+33 dBm	-.33	-.63	-.34
+30 dBm	-.17	-.37	-.20

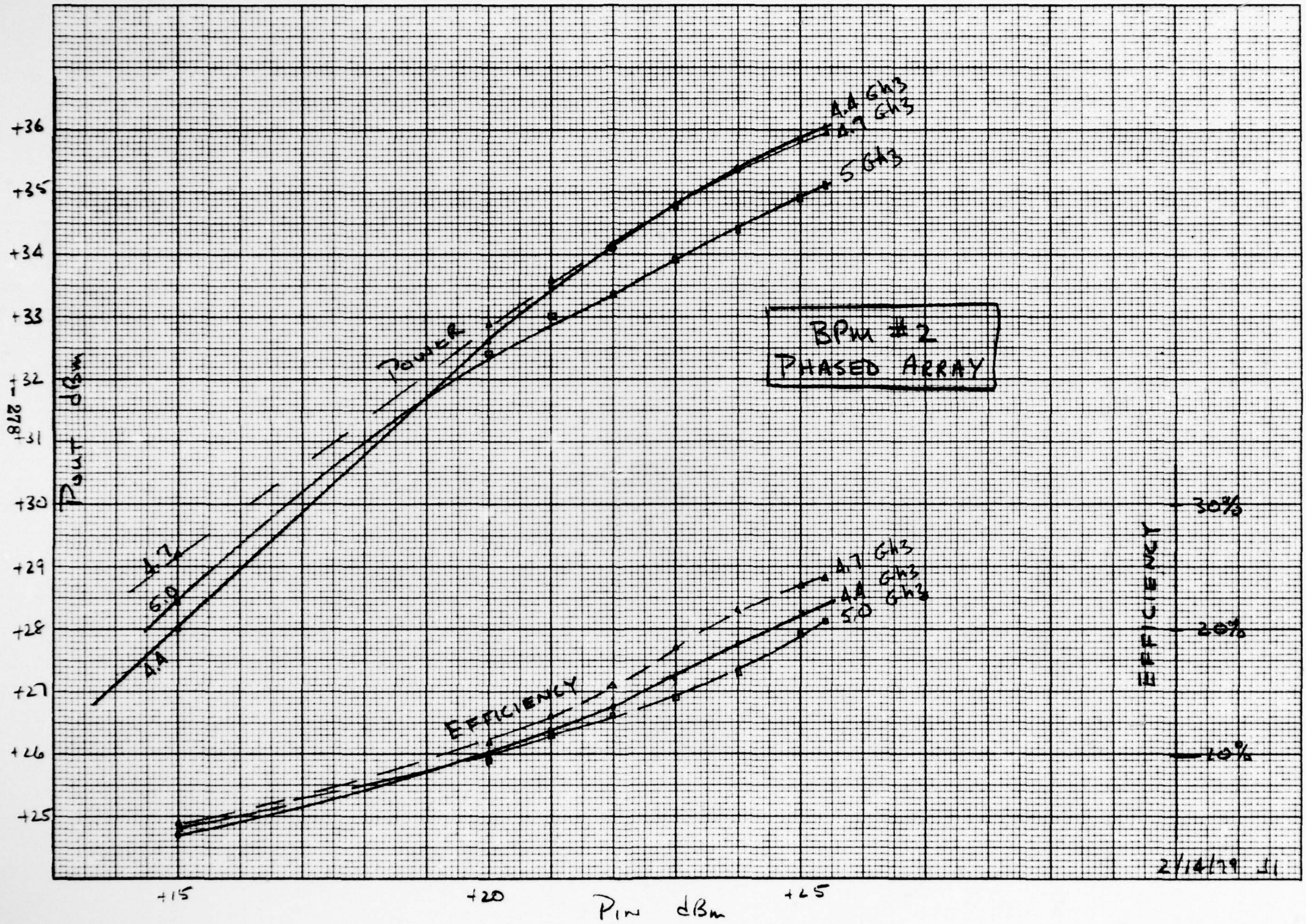
DRAWING NUMBER

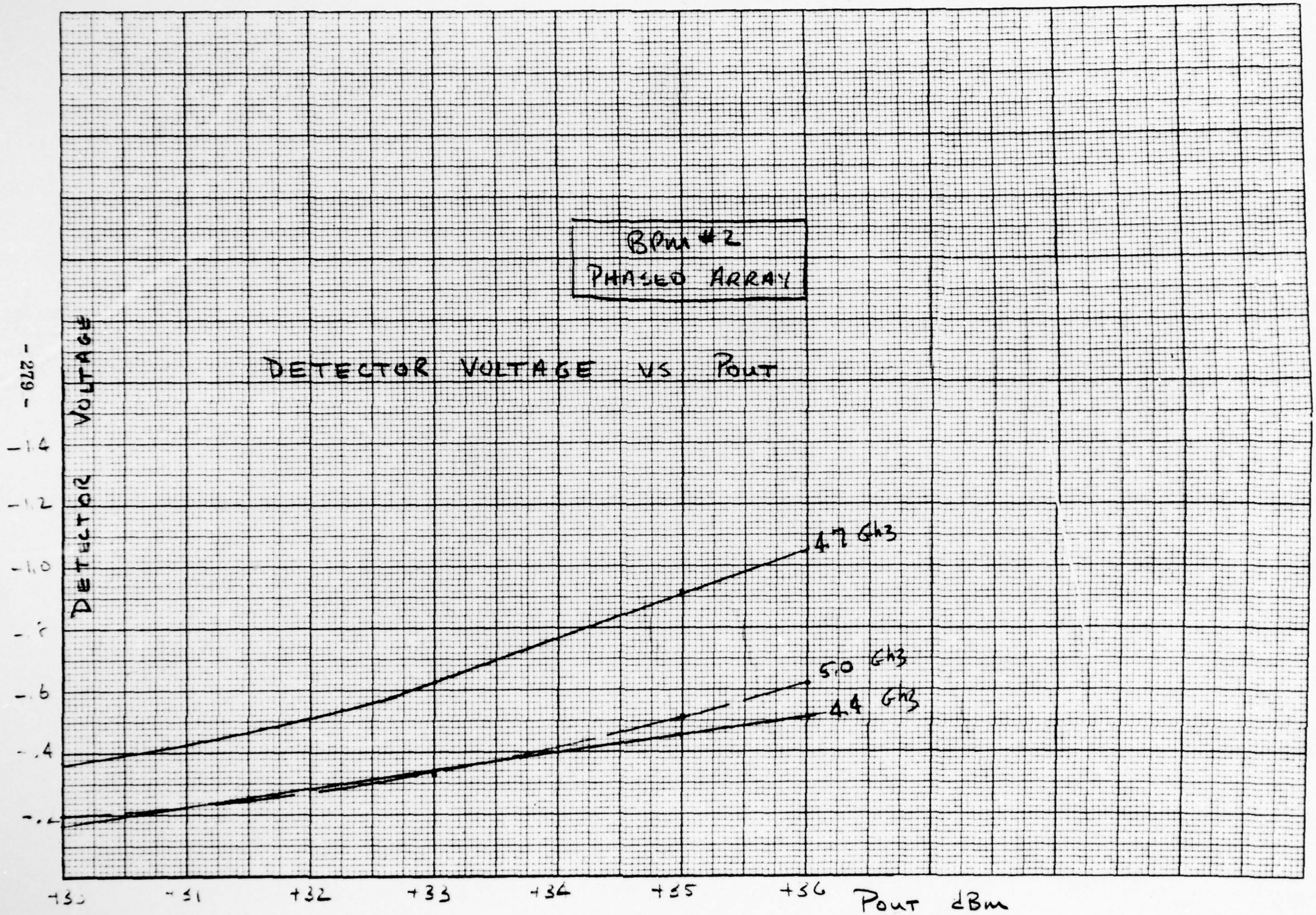
ITT DEFENSE COMMUNICATIONS DIVISION NUTLEY, NEW JERSEY

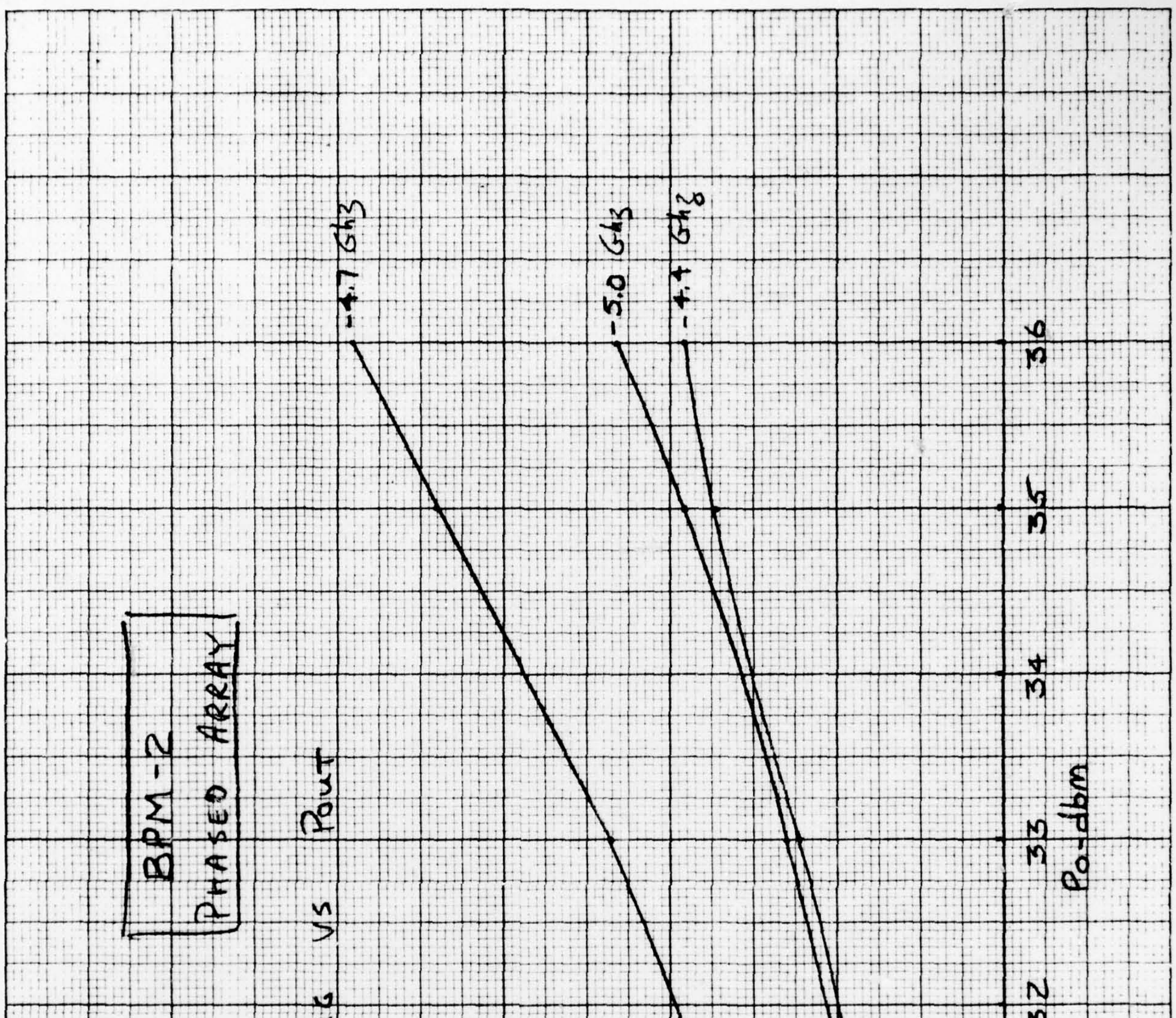
TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION 2 PLACE	3 PLACE	ANGLES	PHASED ARRAY AMPL'S
USED ON		CODE IDENT. NO. 28528	DWG. A SIZE	
PREPARED BY	DATE			
CHECKED BY	DATE			SHEET

D5215 A REV. 6/73


PHASED ARRAY BPM #2
FREQ - GHz
POWER OUTPUT
4.4 GHz
4.7 GHz
5.0 GHz
+35.95 dBm
+35.75 dBm
35.1 dBm
Pin = +26.4 dBm
-1 dB
-2 dB
-3 dB
-4 dB
-5 dB
J.I. 2/8/79

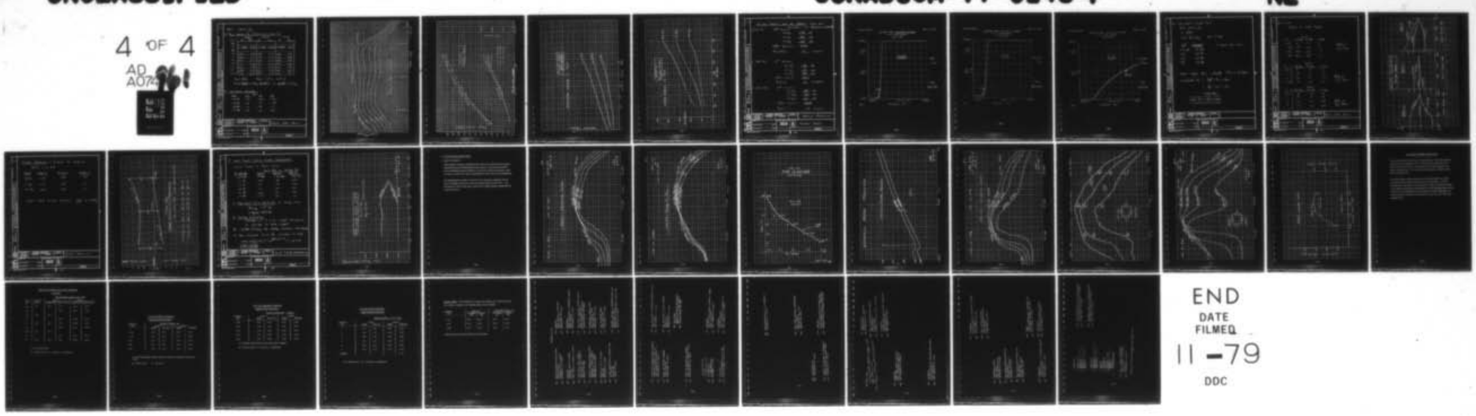

BPm #2
PHASED ARRAY
POWER
EFFICIENCY
4.4 Ghz
4.7 Ghz
5 Ghz
4.7 Ghz
4.4 Ghz
5.0 Ghz
4.7
5.0
4.4
+36
+35
+34
+33
+32
+31
+30
+29
+28
+27
+26
+25
Pout dBm
+15
+20
+25
Pin dBm
30%
20%
10%
EFFICIENCY
2/14/79 JJ


BPM #2
PHASED ARRAY
DETECTOR VOLTAGE VS POUT
DETECTOR VOLTAGE
-1.4
-1.2
-1.0
-.6
-.4
4.7 Ghz
5.0 Ghz
4.4 Ghz
+32
+33
+34
+35
+36
POUT dBm


BPM-2
PHASED ARRAY
METER READING VS POUT
-4.7 Ghz
-5.0 Ghz
-4.4 Ghz
METER (μA)
50
40
30
20
10
0
30
31
32
33
34
35
36
Po-dbm

AD-A074 961 ITT DEFENSE COMMUNICATIONS DIV NUTLEY N J F/G 9/5
PHASED ARRAY ANTENNA AMPLIFIER EXPLORATORY DEVELOPMENT MODEL.(U)
AUG 79 P MUSCIANESI, J IRVINE, J RANGHELLI DAAB07-77-C-0146
UNCLASSIFIED CORADCOM-77-0146-F NL

4 OF 4
AD
A074961



END
DATE
FILMED
11-79
DDC

D
074

1.0 4.5 5.0 5.6 2.8 3.2 3.6 4.0 2.5 2.2 2.0

1.1 1.8

1.25 1.4 1.6

MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

BPM - SER # 3

I] POUT VERSUS PIN / EFFICIENCY VERSUS PIN

PIN	4.4 Ghz Po	4.4 Ghz ITOT	4.7 Ghz Po	4.7 Ghz ITOT	5.0 Ghz Po	5.0 Ghz ITOT
~~+10~~						
+15	-1.0 dBm	2.09a	-.5 dBm	2.08 a	-0.8 dBm	2.02a
~~+18~~						
+20	+3.6	2.09	+3.8	2.10	+3.2	2.03
+21	+4.3	2.10	+4.5	2.10	+3.9	2.04
+22	+5.0	2.10	+5.2	2.10	+4.5	2.05
+23	+5.6	2.07	+5.7	2.12	+5.0	2.00
+24	+6.2	2.04	+6.1	2.10	+5.6	1.98
+25	+6.45	2.04	+6.6	2.09	+6.0	1.95
+25.4	+6.5	2.05	+6.8	2.10	+6.2	1.97

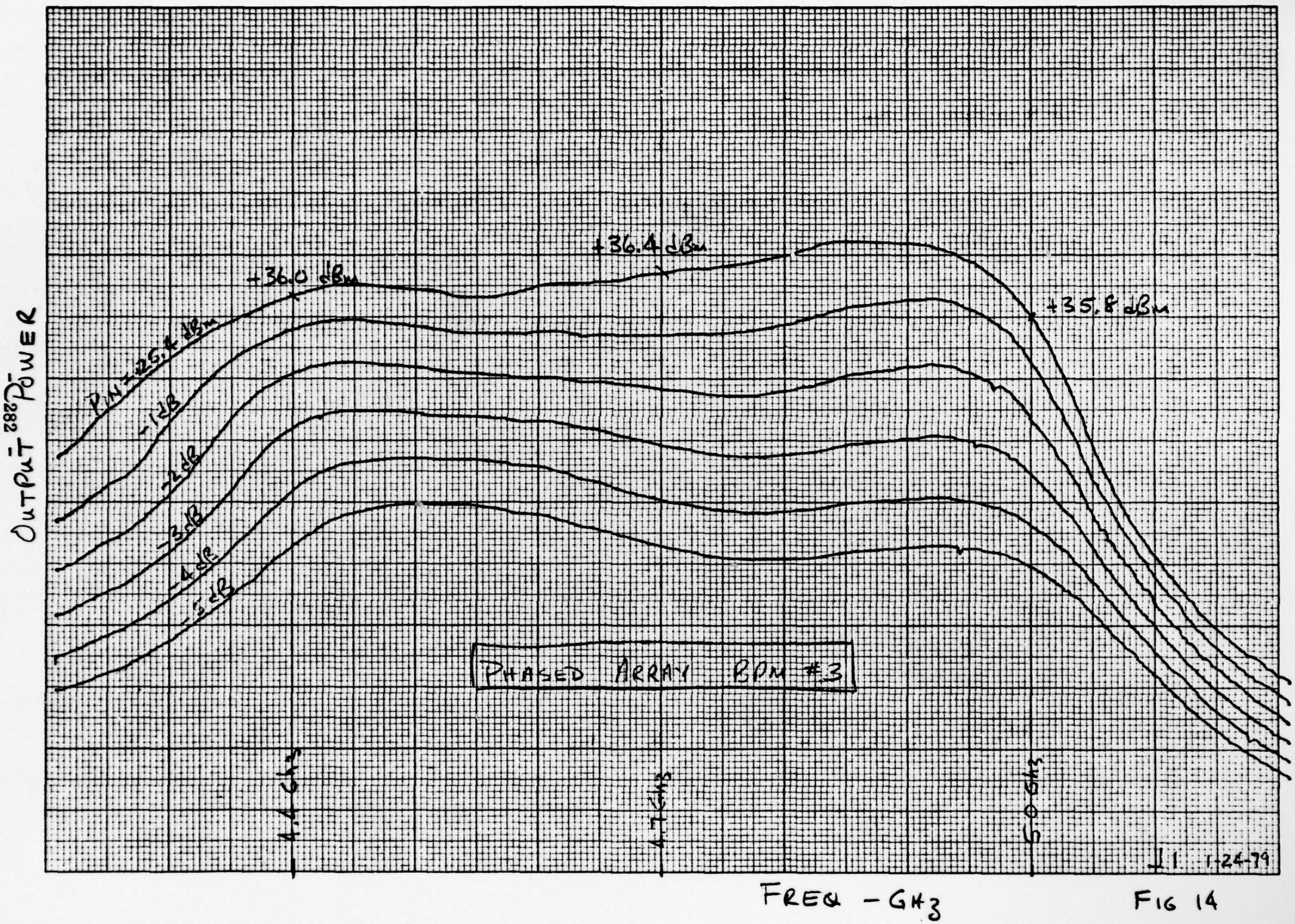
VDS = 8.5 v   ITOT = 2.08 a no drive

CALIB = 29.5 dB at 4.4 Ghz, 29.6 dB at 4.7, 29.6 dB at 5.0 Ghz

II] DETECTOR VOLTAGE

Pout	VDET 4.4	4.7	5.0
+36 dBm	-.54 V	-.86 V	-1.20 V
+35 dBm	-.43	-.75	-1.04
+33 dBm	-.32	-.54	-.79
+30 dBm	-.20	-.30	-.45

TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION 2 PLACE	3 PLACE	ANGLES	PHASED ARRAY AMPL'S
USED ON		CODE IDENT. NO. 28528	DWG. A SIZE	
PREPARED BY	DATE			
CHECKED BY	DATE			SHEET



+36.0 dBm
+36.4 dBm
+35.8 dBm
PIN = +25.8 dBm
-1dB
-2dB
-3dB
-4dB
-5dB
PHASED ARRAY BPM #3
4.4 GHz
4.7 GHz
5.0 GHz
1-24-79
OUTPUT POWER
FREQ - GHz

FIG 14

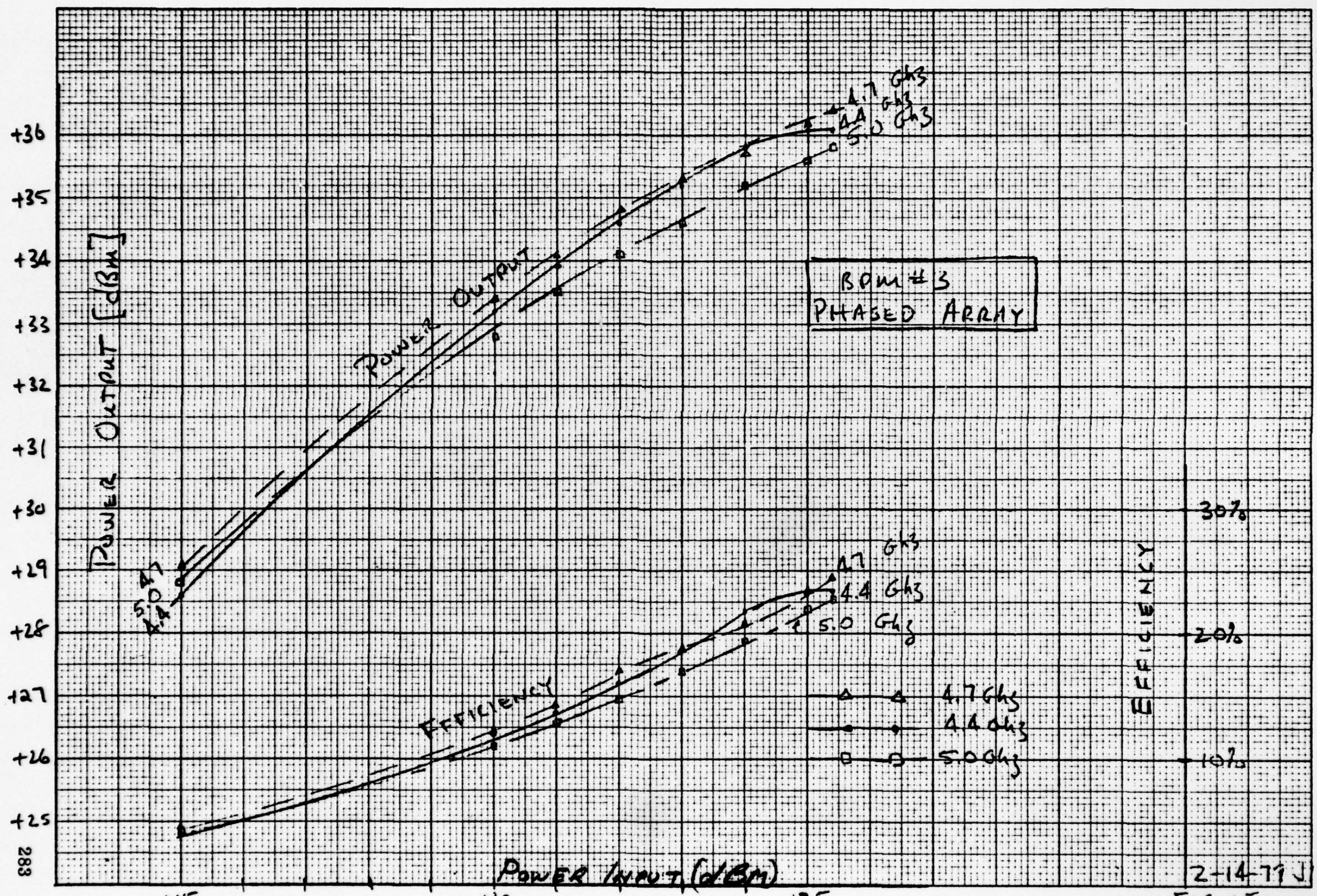
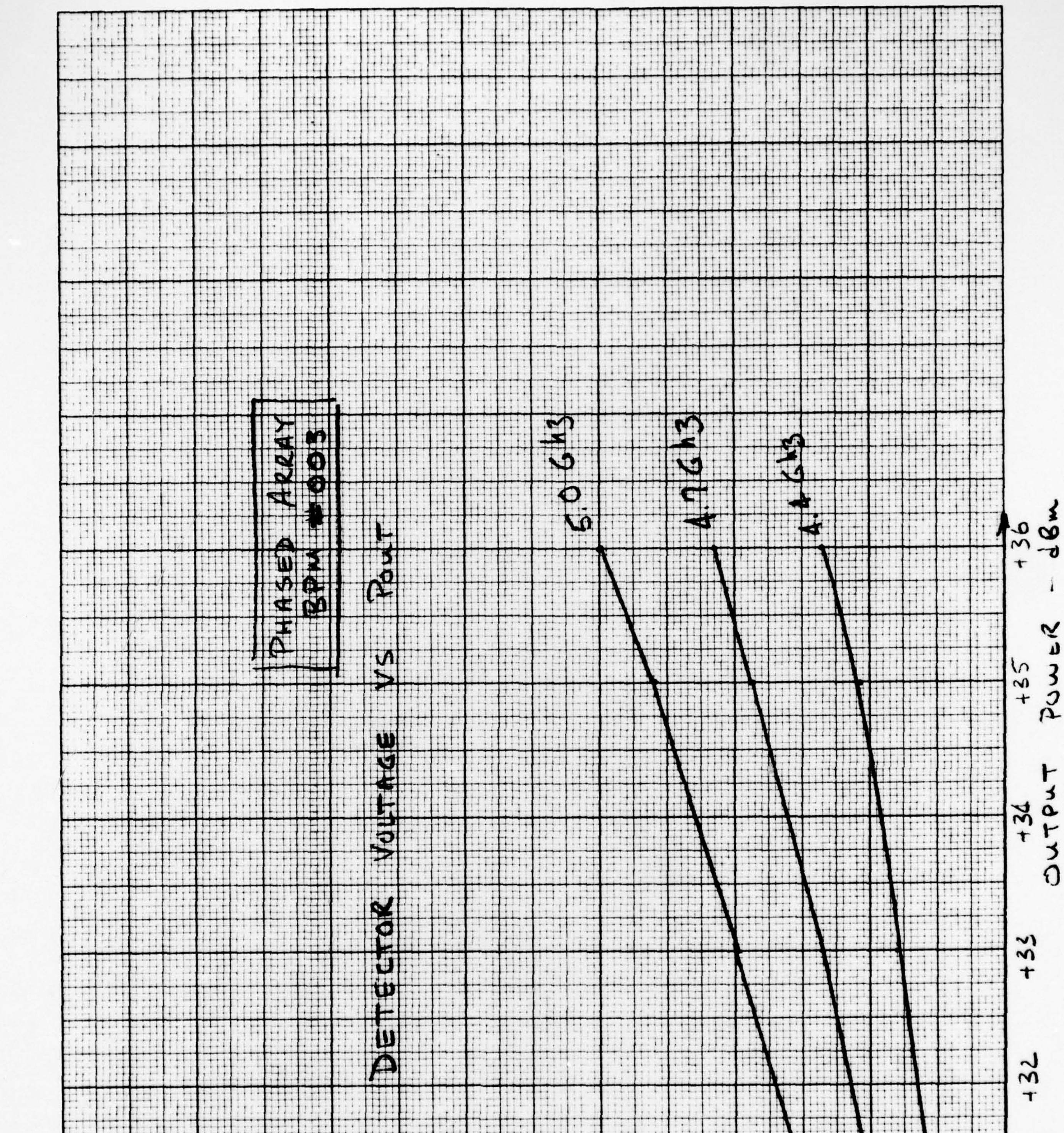
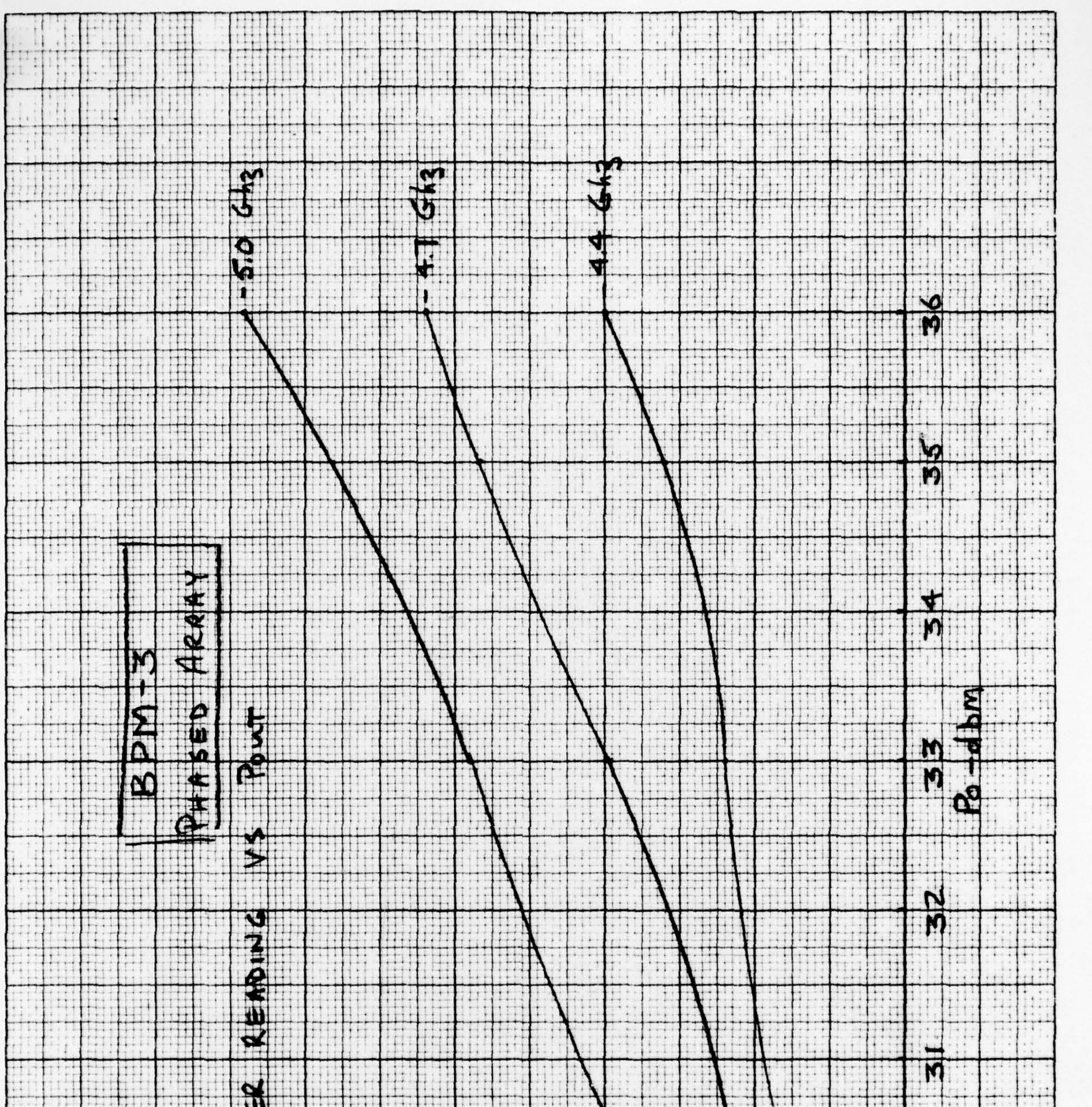

BPM #3
PHASED ARRAY
POWER OUTPUT [dBm]
POWER OUTPUT
EFFICIENCY
POWER INPUT (dBm)
4.7 Ghz
4.4 Ghz
5.0 Ghz
+15
+20
+25
+25
+26
+27
+28
+29
+30
+31
+32
+33
+34
+35
+36
10%
20%
30%
2-14-77 J

FIG 15


DETECTOR VOLTAGE VS Pout
PHASED ARRAY
BPM #003
6.0 Ghz
4.7 Ghz
4.4 Ghz
DETECTOR VOLTAGE
-1.4
-1.2
-1.0
-.8
-.6
-.4
-.2
+30
+31
+32
+33
+34
+35
+36
OUTPUT POWER - dBm


BPM-3
PHASED ARRAY
METER READING VS Pout
5.0 Ghz
4.1 Ghz
4.4 Ghz
METER (mA)
50
40
30
20
10
0
30
31
32
33
34
35
36
Po-dbm

Spurious Radiation OUT OF BPM's - DOES NOT INCLUDE LPF REJECTION (>50dB)

1. BPM #1 2nd Harmonic

4.4 Ghz	-45	dBc
4.7 Ghz	-40	dBc
5.0 Ghz	-40	dBc
Other Spurious	NONE	
Parasitics	✓	complies

2. BPM #2 2nd Harmonic

4.4 Ghz	-38	dBc
4.7 Ghz	-42	dBc
5.0 Ghz	-42	dBc
Other Spurious	NONE	
Parasitic	✓	Complies

3 BPM #3 2nd Harmonic

4.4 Ghz	-40	dBc
4.7 Ghz	-40	dBc
5.0 Ghz	-41	dBc
Other Spurious	NONE	
Parasitics	✓	Complies

DRAWING NUM

ITT DEFENSE COMMUNICATIONS DIVISION NUTLEY, NEW JERSEY

TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION 2 PLACE	3 PLACE	ANGLES	SPURIOUS RADIATION
USED ON	CODE IDENT. NO. 28528	DWG. SIZE A	PHASED ARRAY	
PREPARED BY DATE				
CHECKED BY DATE				SHEET

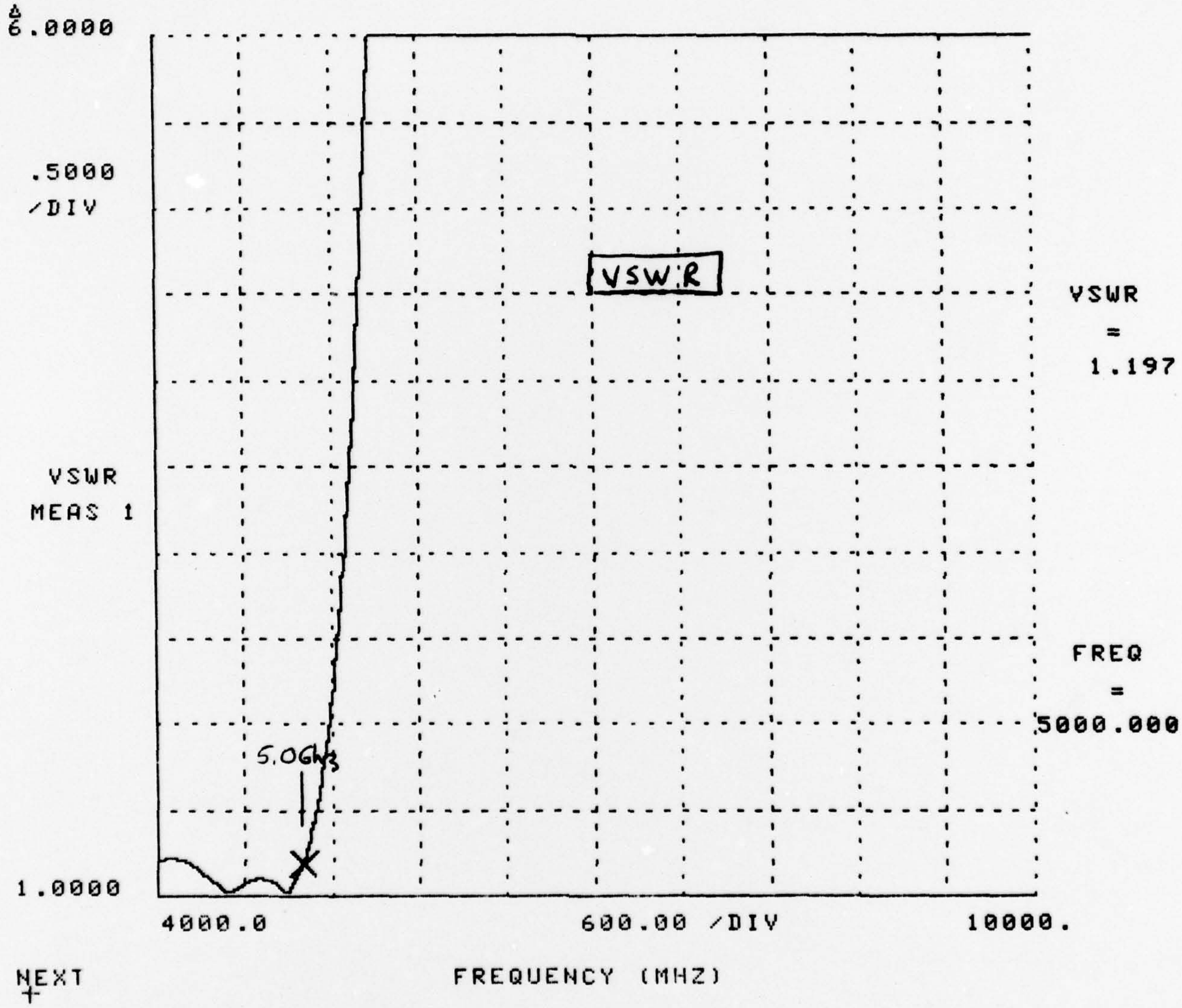
D5215 A REV. 5/73

PHASED ARRAY JAN 31 1979

UNIFORM TUBES LOW PASS FILTERS

UT-L1-250-5000-9

SER # 002



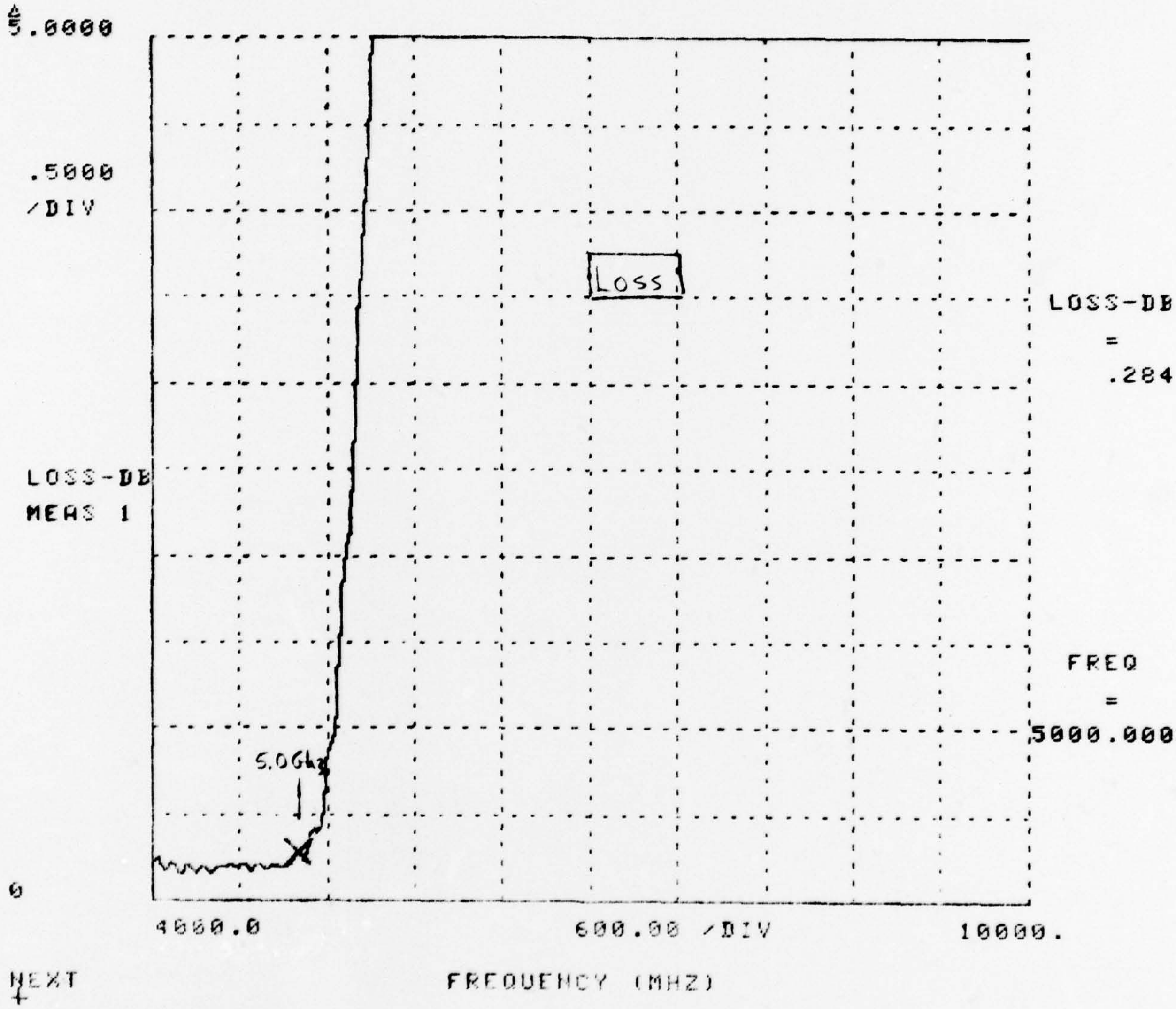
PHASED ARRAY

JAN 31 1979

UNIFORM TUBES LOW PASS FILTERS

UT-L1-250-5000-9

SER # 002

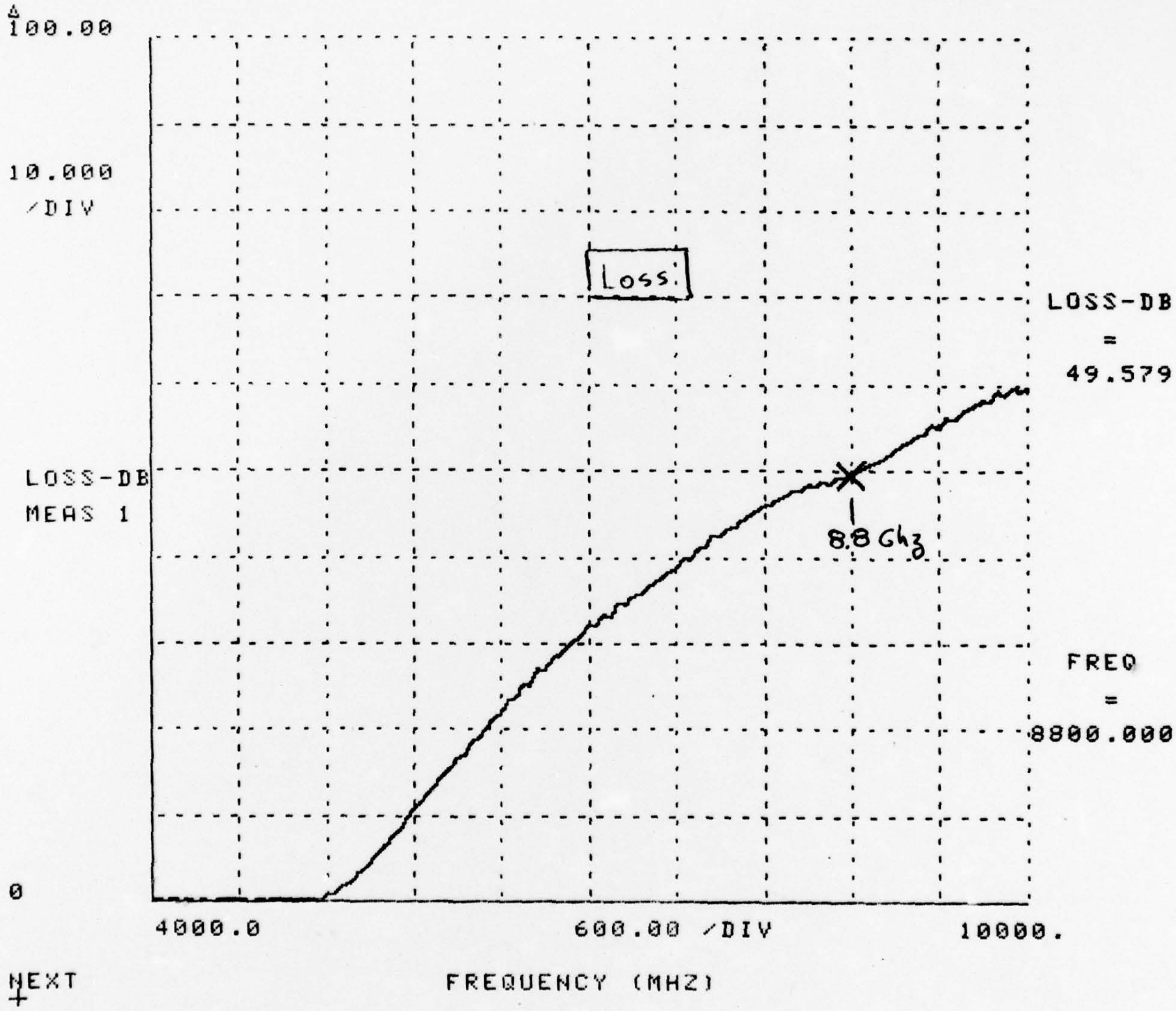


PHASED ARRAY JAN 31 1979

UNIFORM TUBES LOW PASS FILTERS

UT-L1-250-5000-9

SER # 002



IV THIRD ORDER INTERCEPT POINT

BPM SER # 2

V_{DS} 8.5V

FREQ 4.71 Ghz $\Delta f = 3$ mhz

P_{IN}*	IMR(dBc)
+7.4 dBm	-47 dBc
+6.4	-50 dBc
+5.4	-52 dBc
+4.4	-54 dBc

* power per tone

Small Signal Gain 14.2 dB (P_{IN} < +15 dBm)

$$\text{INTERCEPT PT} = \frac{IMR}{2} + P_{IN} + \text{Gain}$$

$$= \frac{50}{2} + 6.4 + 14.2$$

$$= 45.6 \text{ dBm}$$

$$\boxed{\text{Int Pt} = +45.6 \text{ dBm}}$$

TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION 2 PLACE	3 PLACE	ANGLES

USED ON	CODE IDENT. NO.	DWG. SIZE	
PREPARED BY DATE	28528	A	
CHECKED BY DATE			SHEET

III] AM/PM

PHASE VS INPUT POWER

PHASE

PIN	4.4 Ghz	4.7 Ghz	5.0 Ghz
+25.4	0	0	0
− 1 dB	+ 2°	−1.0°	0°
− 2 dB	+3.6°	− 4.0°	−.1°
− 3 dB	+4.0°	− 4.4°	−.2°

BPM 1

V_{DS} = 8.4 v

PHASE

PIN	4.4 Ghz	4.7 Ghz	5.0 Ghz
+25.4	0	0	0
− 1	+.3°	−0°	+.8°
− 2	+.4	−.5	+1.6
− 3 dB	+.5	−1.5	+2.3

BPM 2

V_{DS} = 8.5 V

PHASE

PIN	4.4 Ghz	4.7 Ghz	5.0 Ghz
+25.4	0	0	0
− 1	+.8°	−1.7°	+2.0
− 2	+1.8	− 2.3	+ 3.8
− 3	+1.9	− 2.3	+5.4

BPM 3

V_{DS} = 8.48 V

DRAWING NUMBER

ITT DEFENSE COMMUNICATIONS DIVISION NUTLEY, NEW JERSEY

TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION 2 PLACE	3 PLACE	ANGLES	PHASED ARRAY AMPL'S

USED ON

PREPARED BY DATE

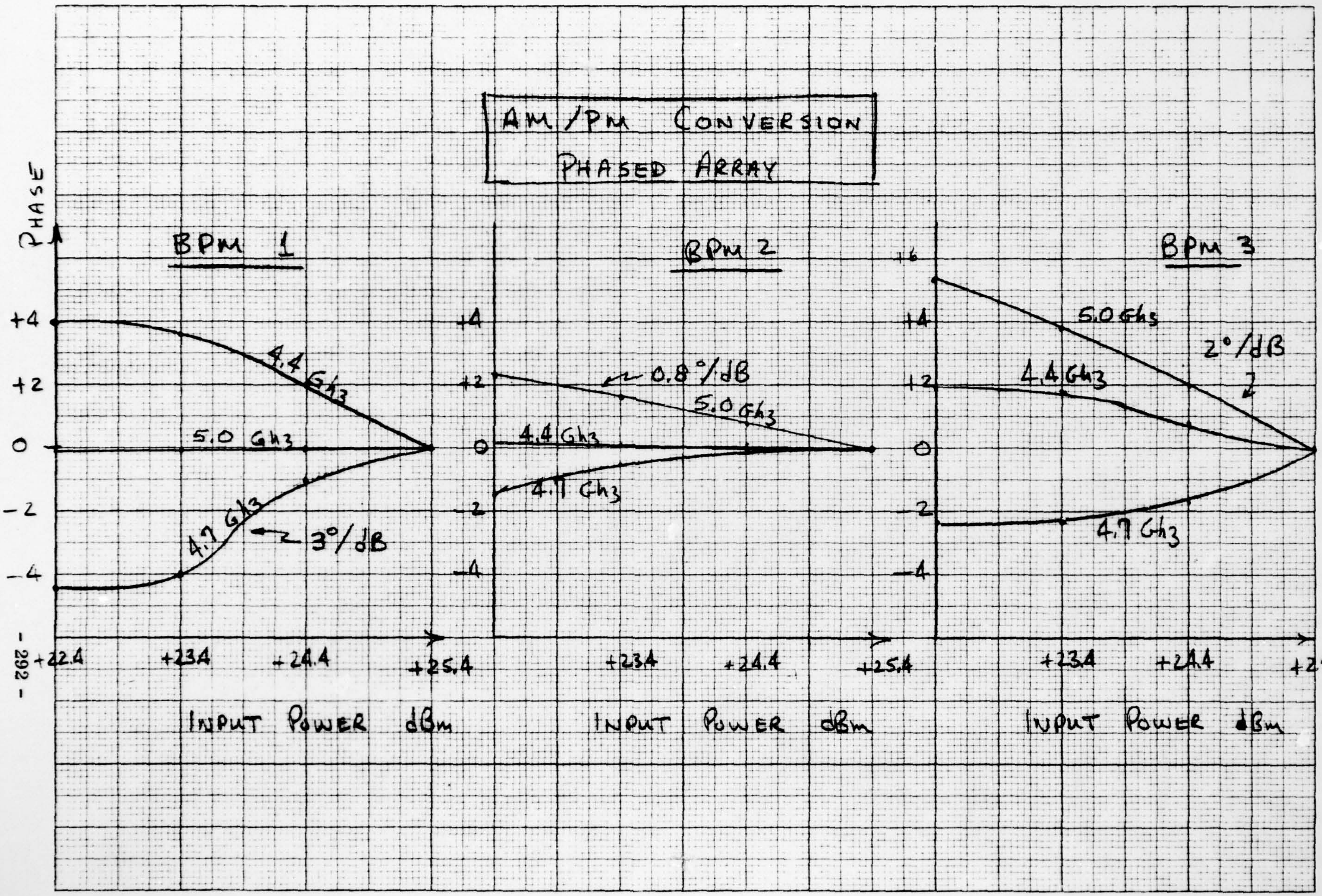
CHECKED BY DATE

CODE IDENT. NO. 28528

DWG. A SIZE

SHEET

D8216 A REV. 8/73


AM/PM CONVERSION
PHASED ARRAY
PHASE
BPM 1
BPM 2
BPM 3
+4
+2
0
-2
-4
+6
4.4 Ghz
5.0 Ghz
4.7 Ghz
3°/dB
0.8°/dB
2°/dB
+22.4
+23.4
+24.4
+25.4
INPUT POWER dBm

PHASE TRACKING — MODULE TO MODULE

BPM's 1, 2, & 3

FREQ	2 REL 1	3 REL 2	3 REL 1
4.4 Ghz	+29°	-44°	-15°
4.7 Ghz	+27°	-34°	-7°
5.0 Ghz	+46°	-44°	+2°

WORST CASE PHASE TRACKING ±23° at 5.0 Ghz

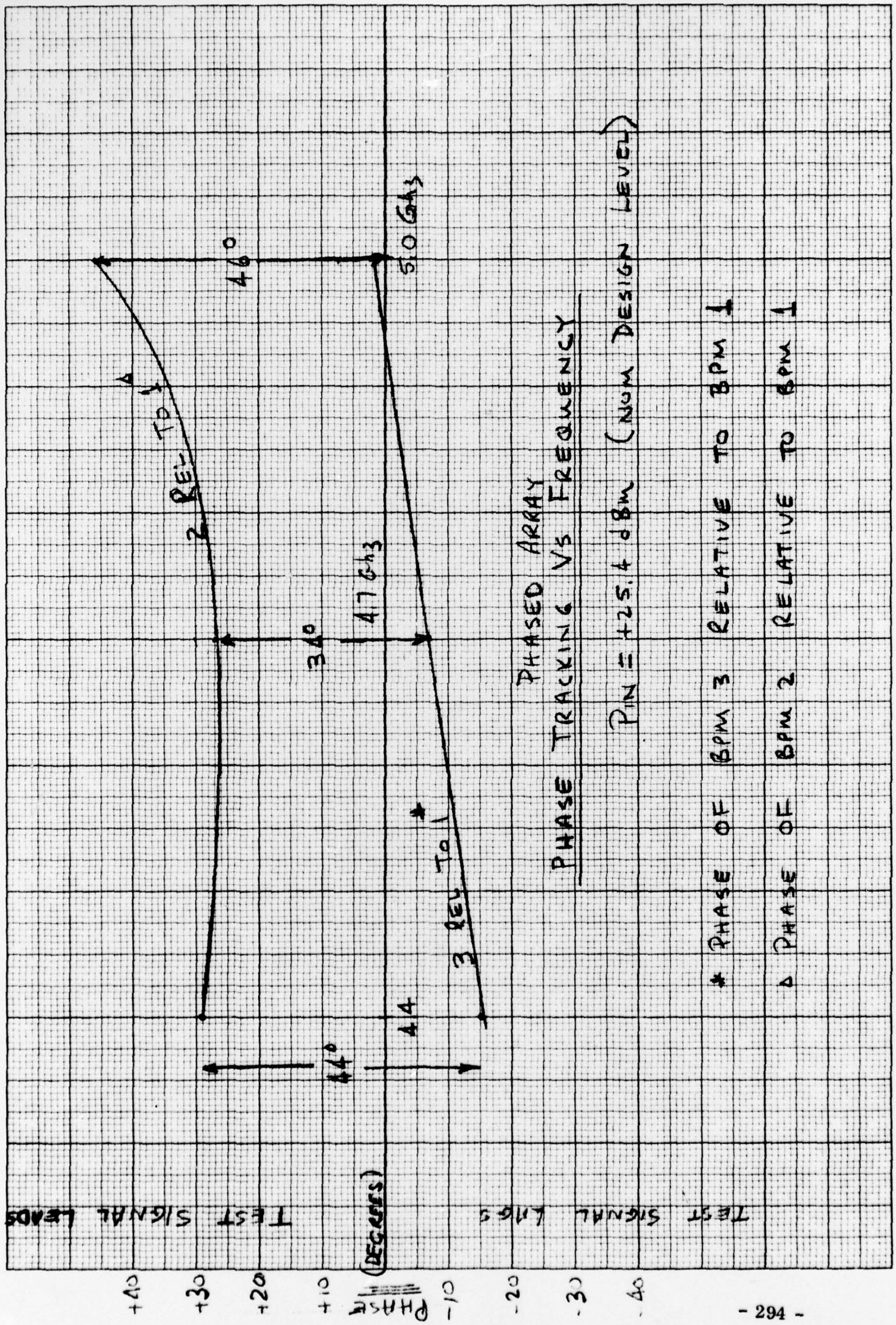
DRAWING NUM

ITT DEFENSE COMMUNICATIONS DIVISION NUTLEY, NEW JERSEY

TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION 2 PLACE	DECIMAL DIMENSION 3 PLACE	ANGLES	PHASE TRACKING

USED ON	CODE IDENT. NO.	DWG. SIZE	
PREPARED BY / DATE	28528	A	
CHECKED BY / DATE			SHEET

D5215 A REV. 5/73



PHASED ARRAY
PHASE TRACKING VS FREQUENCY
PIN = +25.4 dBm (NOM DESIGN LEVEL)
* PHASE OF BPM 3 RELATIVE TO BPM 1
Δ PHASE OF BPM 2 RELATIVE TO BPM 1
2 REL TO 1
3 REL TO 1
4.6°
5.0 GHz
3.4°
4.7 GHz
4.4°
4.4
TEST SIGNAL LEADS
TEST SIGNAL LAGS
PHASE (DEGREES)
+40
+30
+20
+10
-10
-20
-30
-40

V NOISE POWER & NOISE FIGURE DEGRADATION

1) NOISE POWER VS DRIVE LEVEL

PIN @4.7 Ghz	BPM #1	BPM #2	BPM #3
	NOISE PWR IN 775 Khz BW		
+25.4 dBm	-55 dBm	-59 dBm	-55 dBm
-1 dB	-52.5	-59	-57.5
-2 dB	-51	-59	-59
-3 dB	-51.7	-59	-59
-4 dB	-51.5	-59	-59
-5 dB	-51.5	-59	-59

2) Equivalent Noise Bandwidth of 70 mhz Filter

$$BW_{-3dB} = 775 \text{ Khz}$$

$$10 \log BW = 58.9 \text{ dB}$$

3) SET-up Calibration

-55 dBm at IF Filter output corresponds to -86 dBm at BPM output

4) $-86 \text{ dBm} / 775 \text{ Khz} \Rightarrow -86 \text{dBm} - 58.9 \text{dB} = -144.9 \text{ dBm/Hz}$

5) FOR ANTENNA TX TO RX ISOLATION OF 30 dB

$$NFD = 10 \log \left[1.41 \times 10^{-17} + 10^{\frac{1}{10}(P_{NOISE} - I)}\right] + 168.5 \text{ dB}$$

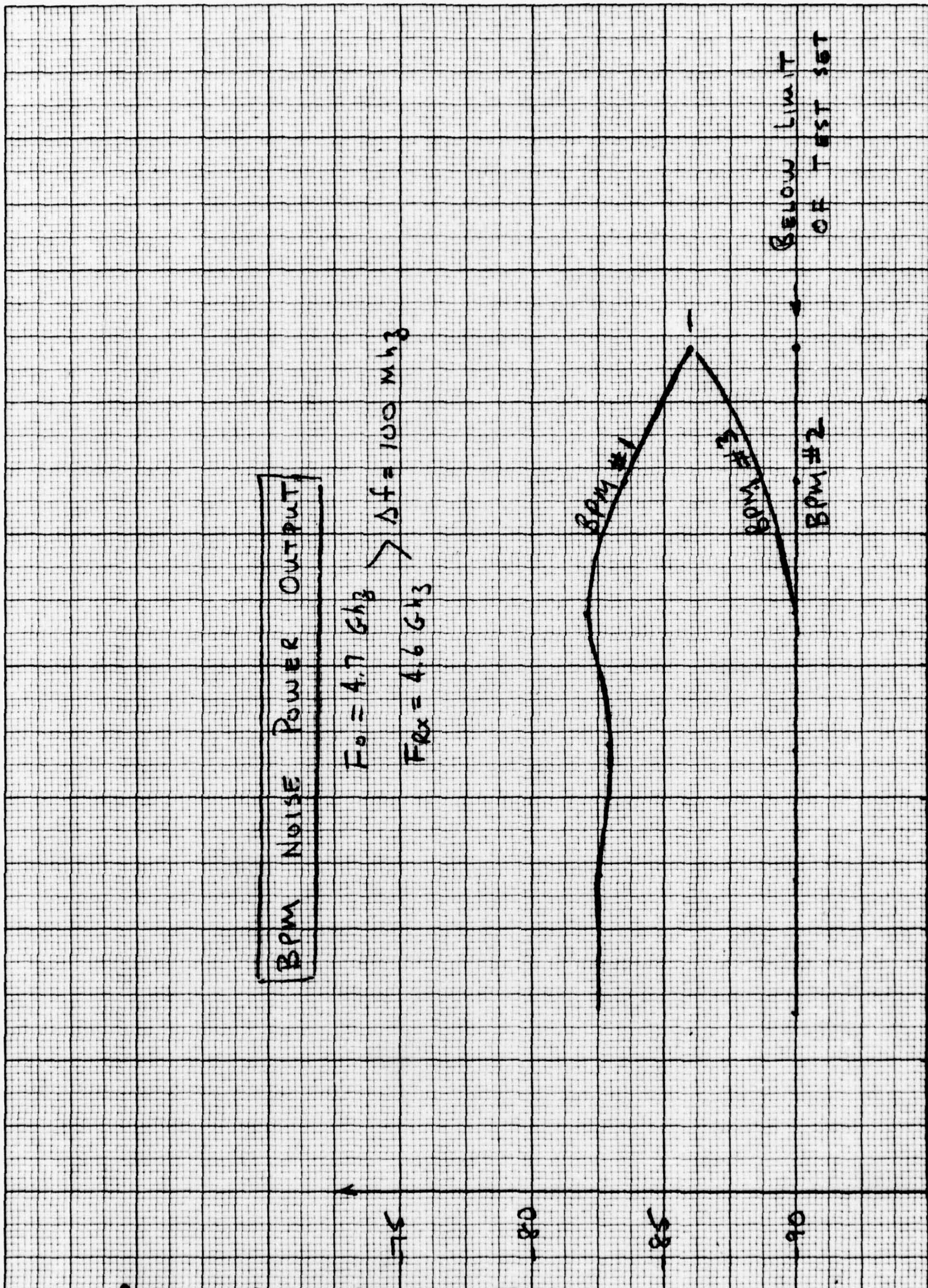
$$\boxed{NFD = 0.89 \text{ dB}}$$

TOLERANCES UNLESS OTHERWISE SPECIFIED	DECIMAL DIMENSION 2 PLACE	3 PLACE	ANGLES	NOISE FIGURE DEGRADATION
USED ON	CODE IDENT. NO. 28528	DWG. A SIZE		
PREPARED BY DATE				
CHECKED BY DATE				SHEET

ITT DEFENSE COMMUNICATIONS DIVISION NUTLEY, NEW JERSEY

DRAWING NUMBER

D5215 A REV. 8/73



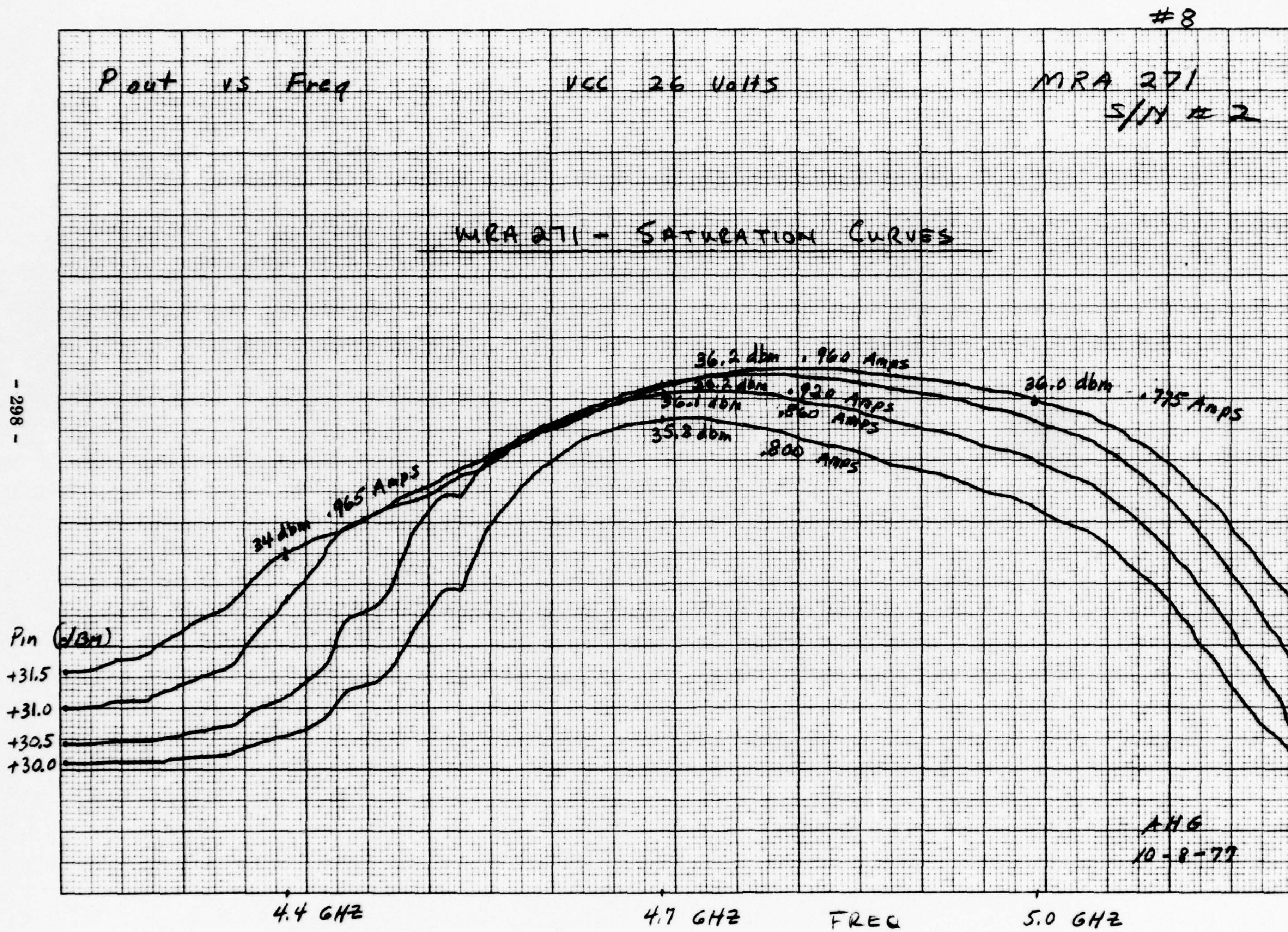
BPM NOISE POWER OUTPUT
$F_o = 4.7$ Ghz
$F_{Rx} = 4.6$ Ghz
$\Delta f = 100$ Mhz
BPM #1
BPM #3
BPM #2
BELOW LIMIT OF TEST SET
+20
+21
+22
+23
+24
+25
INPUT DRIVE - dBm
75
80
85
90
NOISE POWER - dBm/775 KHz

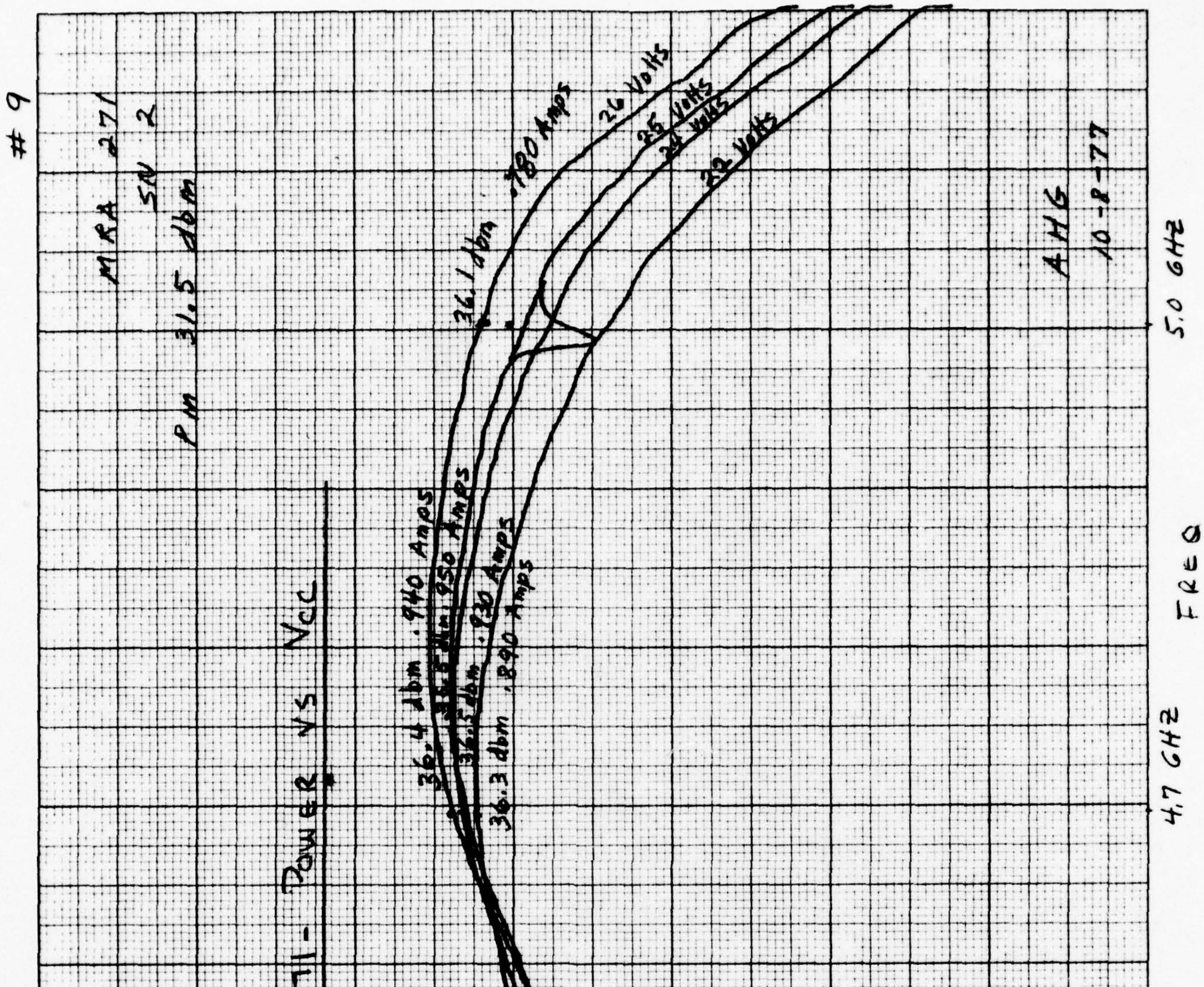
B EXTENDED AMPLIFIER TESTS

2. Bipolar Transistors

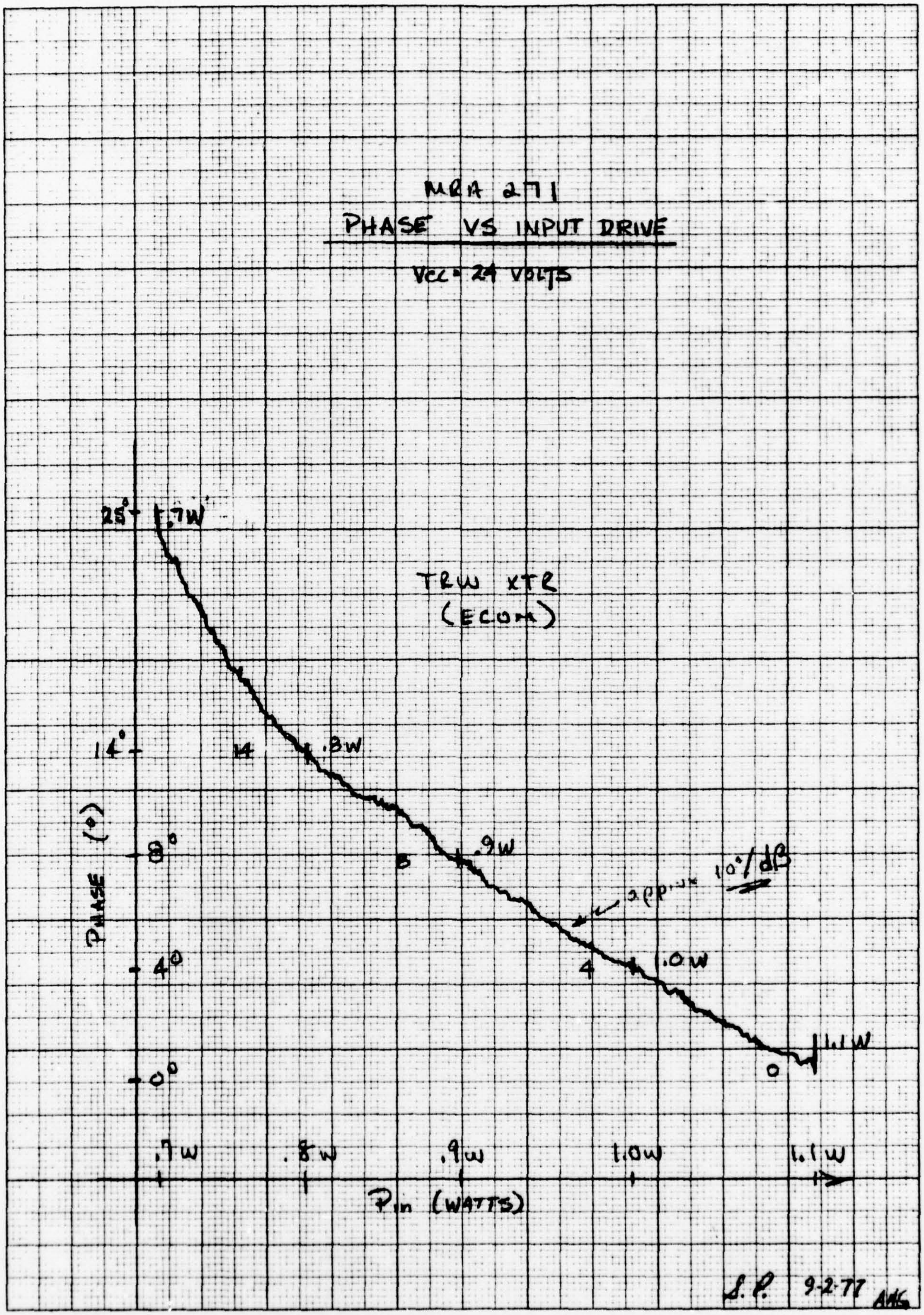
Silicon bipolar transistors manufactured by TRW were evaluated for this system application during the initial phases of this contract. Several characteristics such as bandwidth and gain sensitivity to drive level, AM/PM conversion, phase tracking, and noise power output were identified as risk areas for this application.

The following data was taken on the MRA 271 (5 cell power transistor) and the MRA 272 (single cell driver) as well as combined MRA 271's and 272's. The last graph is a plot of noise power output of the complete bipolar amplifier (BPM) versus drive level.

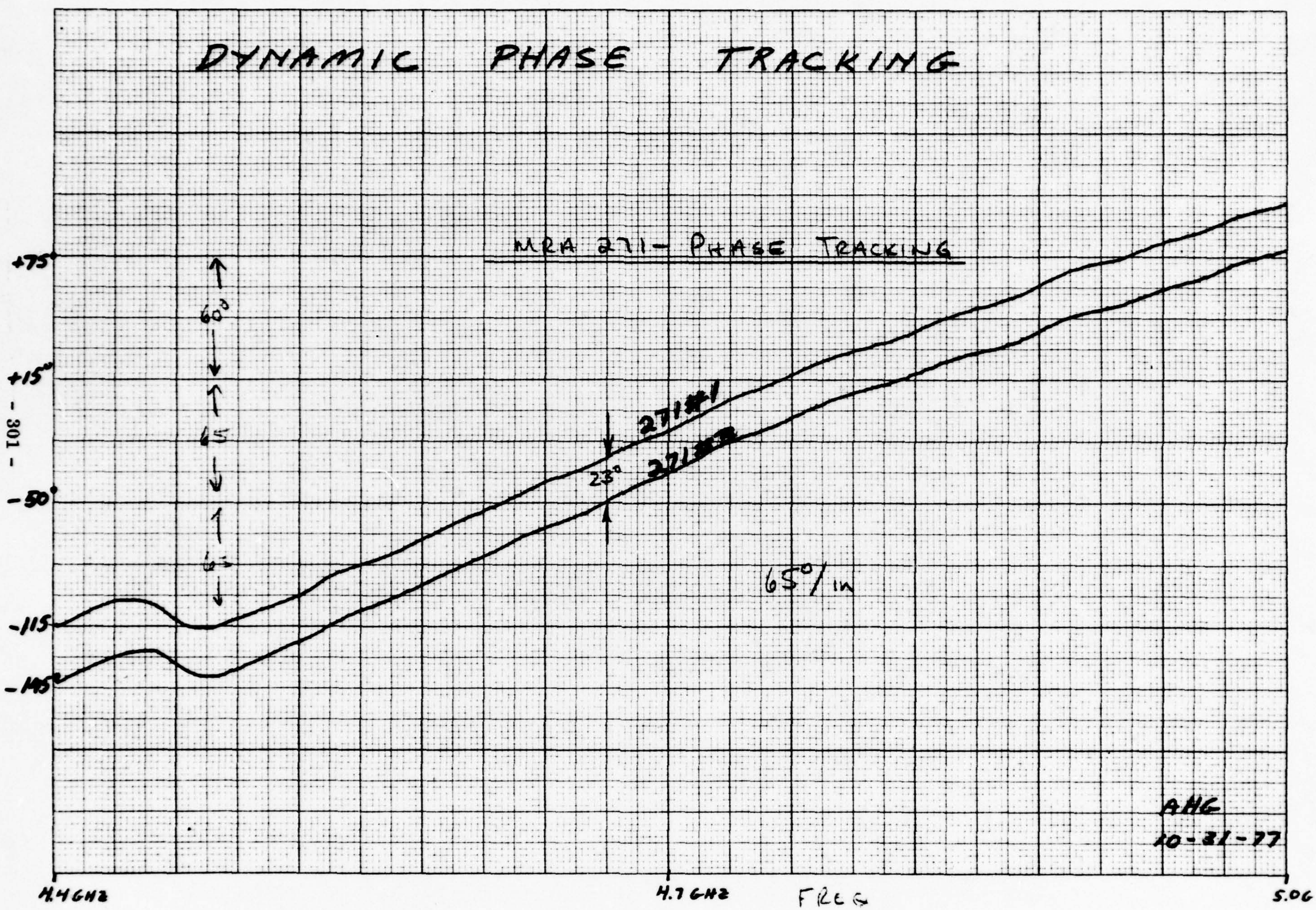

#8
Pout vs Freq
VCC 26 Volts
MRA 271
S/N # 2
MRA 271 - SATURATION CURVES
36.2 dbm .960 Amps
36.0 dbm .775 Amps
.920 Amps
36.1 dbm .860 Amps
35.8 dbm .800 Amps
34 dbm .965 Amps
Pin (dBm)
+31.5
+31.0
+30.5
+30.0
AHG
10-8-77
4.4 GHZ
4.7 GHZ
FREQ
5.0 GHZ



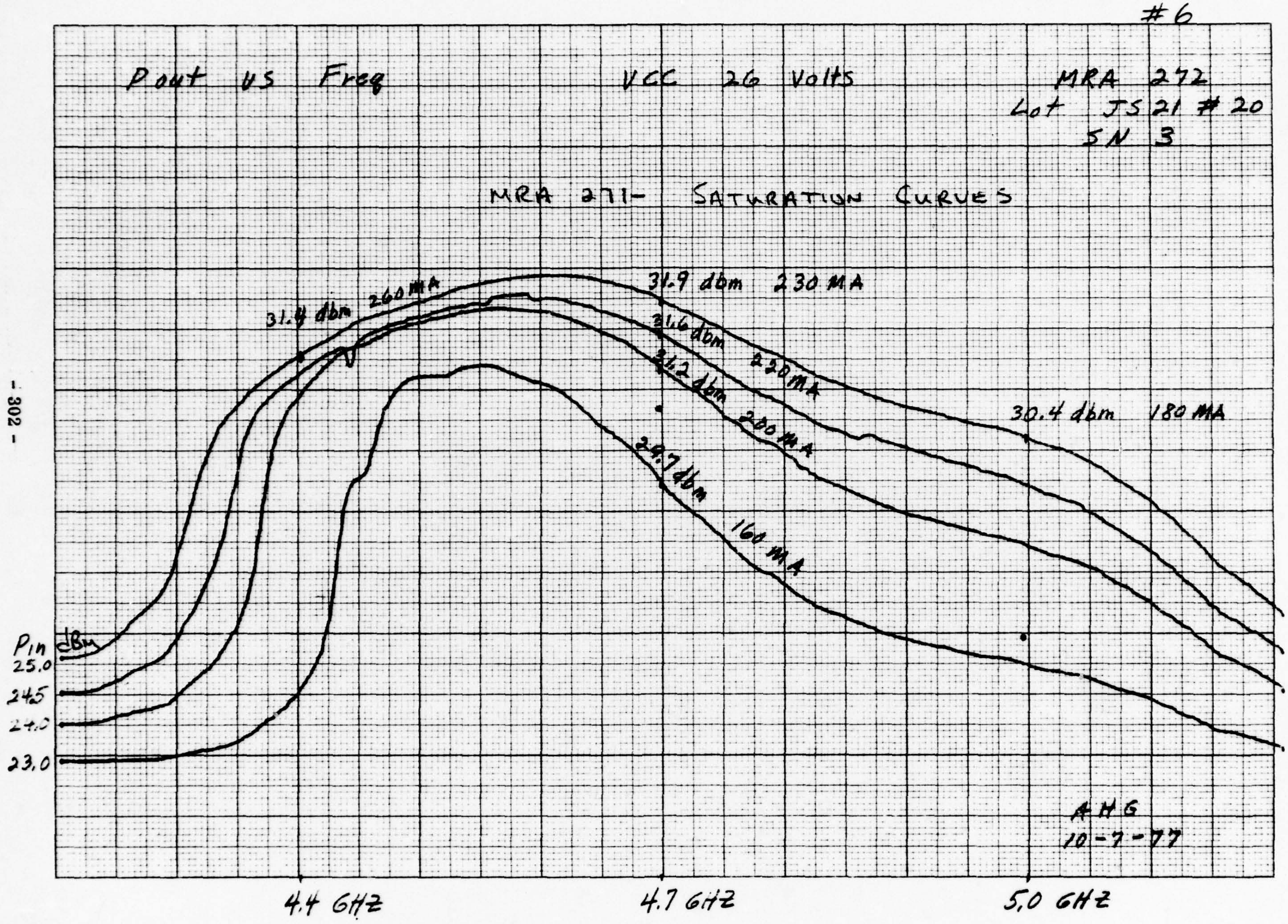
#9
MRA 271
SN 2
Pin 31.5 dbm
Pout vs voltage
MRA 271 - POWER VS Vcc
26 Volts
25 Volts
24 Volts
23 Volts
.980 Amps
36.1 dbm
36.4 dbm .940 Amps
.950 Amps
.930 Amps
36.3 dbm .890 Amps
34.2 dbm .950 Amps
4.4 GHZ
4.7 GHZ
5.0 GHZ
FREQ
AHG
10-8-77

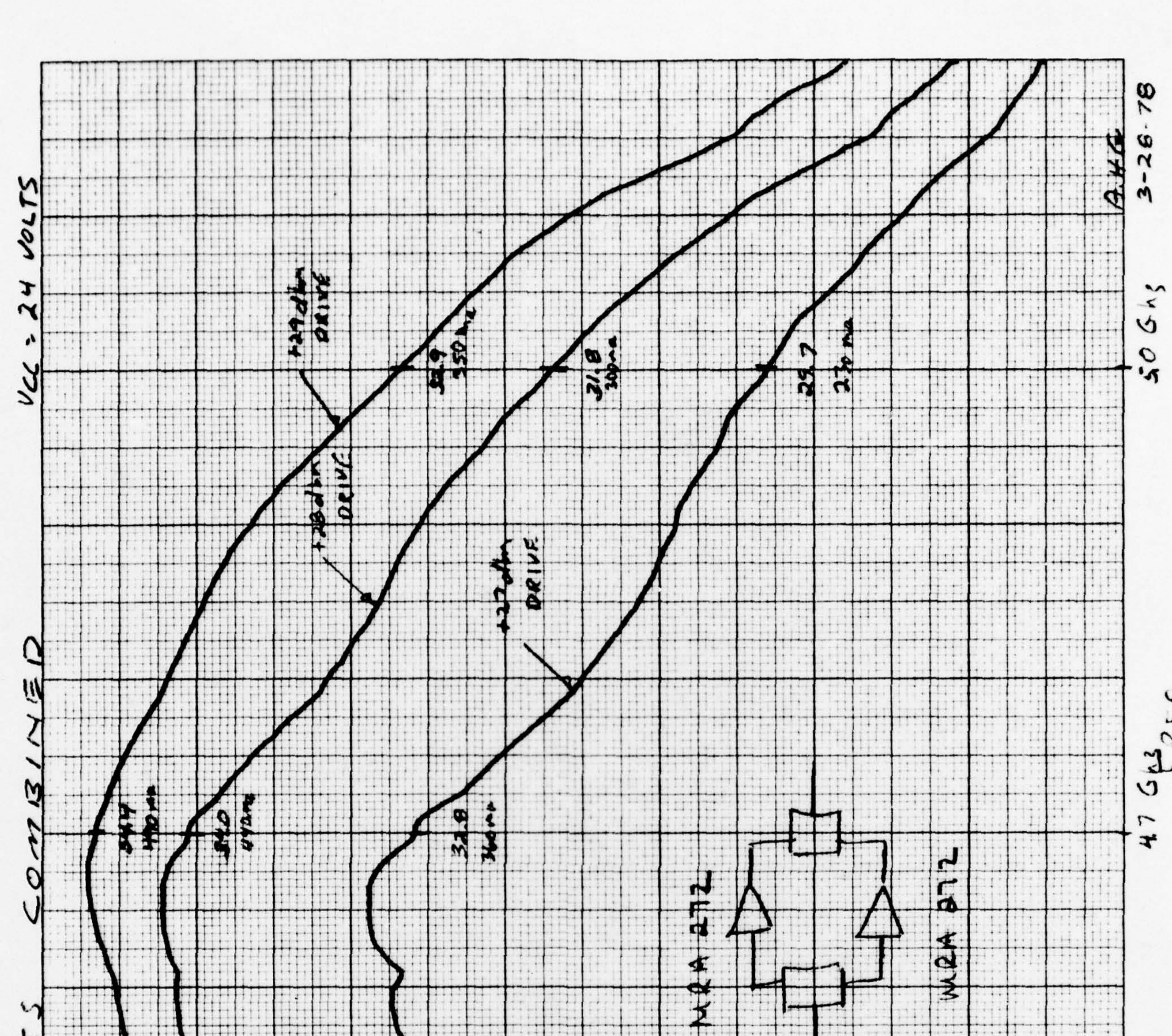


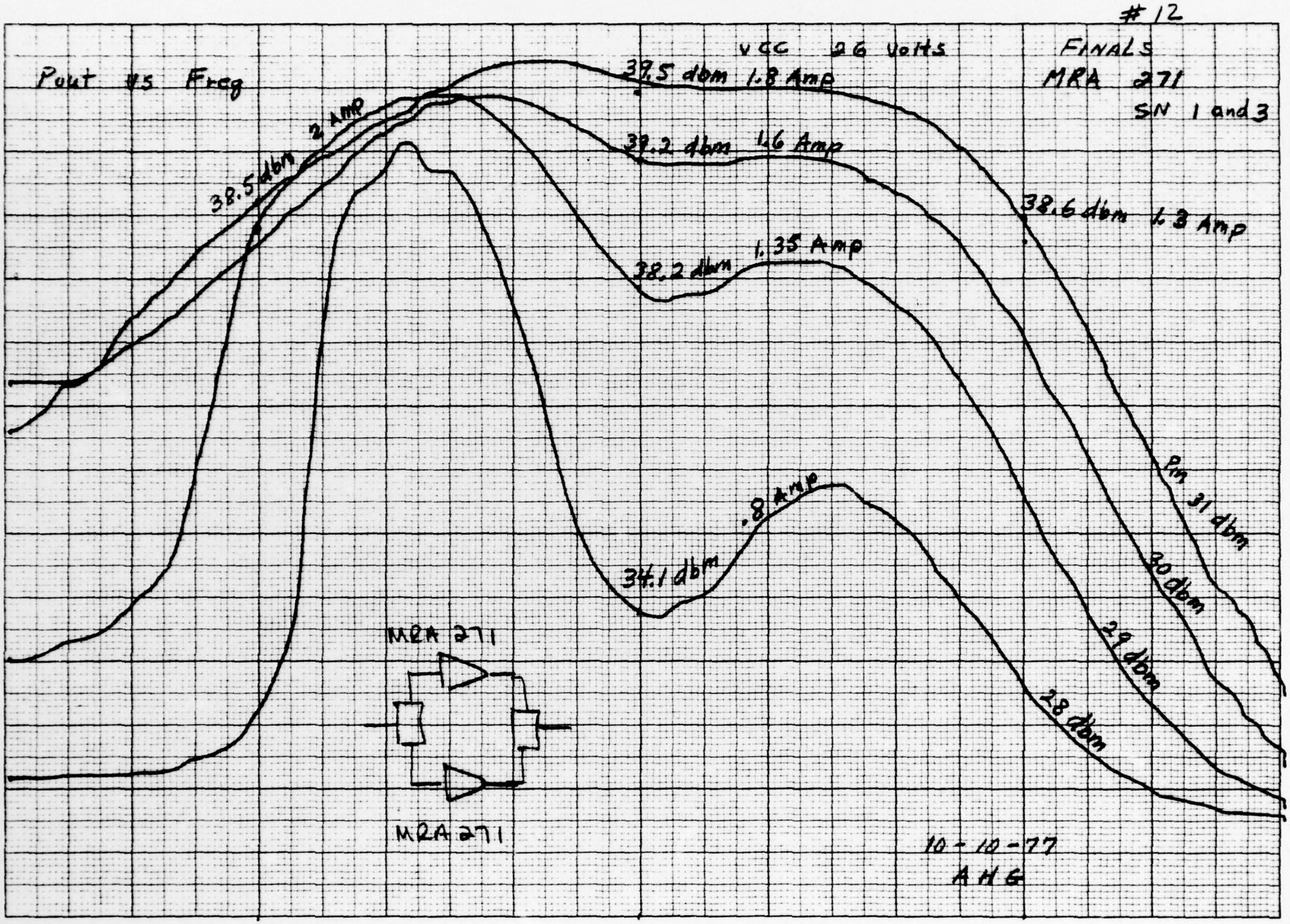
MRA 271
PHASE VS INPUT DRIVE
Vcc = 24 VOLTS
TRW XTR
(ECOM)
25°
.7W
14°
14
.8W
PHASE (°)
8°
8
.9W
approx 10°/dB
4°
4
1.0W
1.1W
0°
0
.7W
.8W
.9W
1.0W
1.1W
Pin (WATTS)
9-2-77



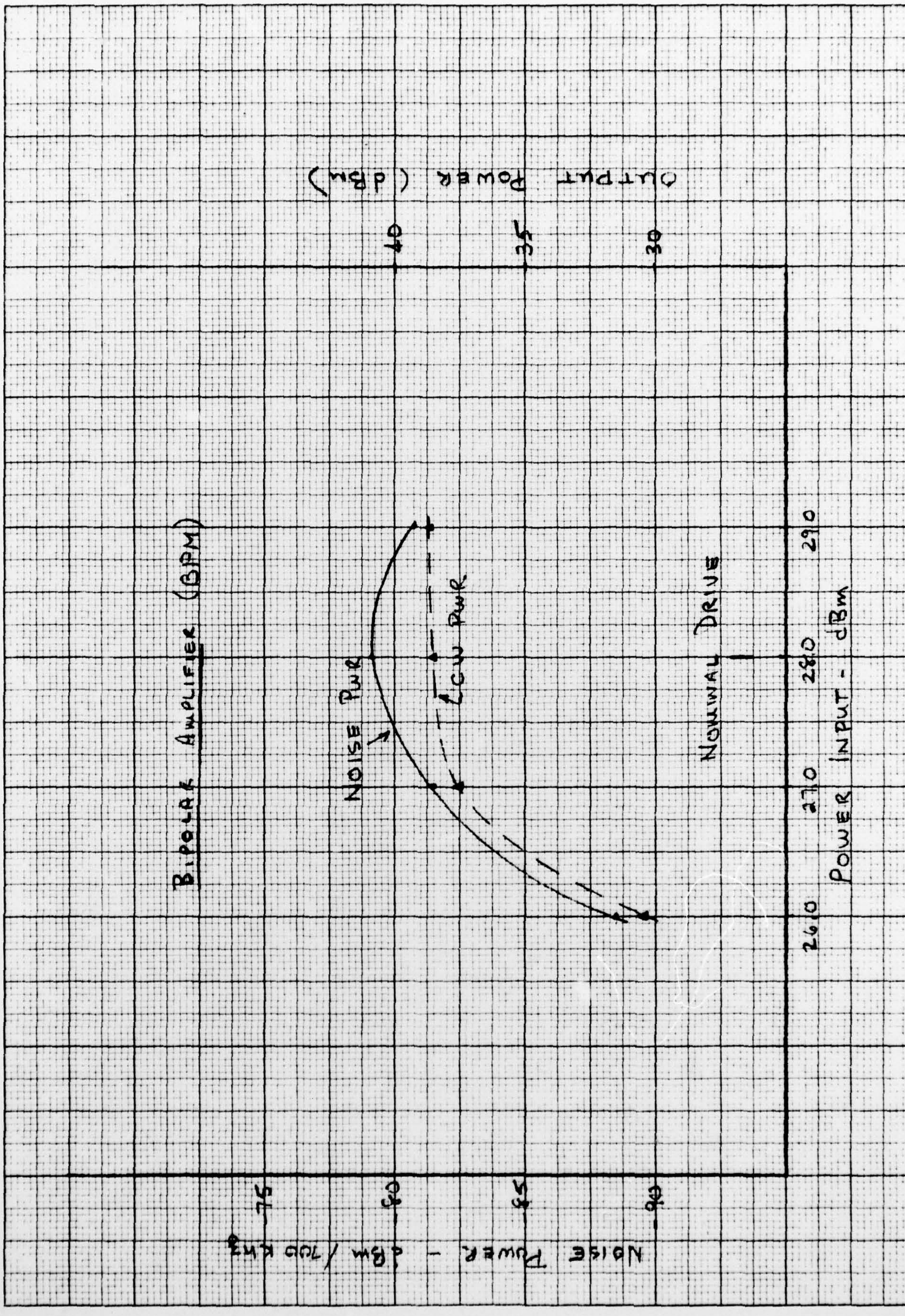
DYNAMIC PHASE TRACKING
MRA 271 - PHASE TRACKING
+75°
+15°
-50°
-115°
-145°
60°
65
65
271#1
271#2
23°
65°/IN
AHG
10-31-77
4.4GHZ
4.7GHZ
FREQ
5.0G


#6
Pout vs Freq
VCC 26 Volts
MRA 272
Lot JS21 #20
SN 3
MRA 271- SATURATION CURVES
31.9 dbm 230 MA
31.4 dbm 260 MA
31.6 dbm 220 MA
31.2 dbm 200 MA
29.7 dbm 160 MA
30.4 dbm 180 MA
Pin dBm
25.0
24.5
24.0
23.0
4.4 GHZ
4.7 GHZ
5.0 GHZ
AHG
10-7-77


BPM DRIVER STAGES COMBINED
VCC = 24 VOLTS
+29 dbm DRIVE
+28 dbm DRIVE
+27 dbm DRIVE
MRA 272
MRA 272
4.4 GHz
4.7 GHz
5.0 GHz
FREQ
A.H.G.
3-26-78



12
Pout #5 Freq
VCC 26 Volts
FINALS
MRA 271
SN 1 and 3
39.5 dbm 1.8 Amp
39.2 dbm 1.6 Amp
38.2 dbm 1.35 Amp
38.5 dbm 2 Amp
38.6 dbm 1.3 Amp
34.1 dbm .8 Amp
Pin 31 dbm
30 dbm
29 dbm
28 dbm
MRA 271
MRA 271
10-10-77
AHG
4.4 GHZ
4.7 GHZ
5.0 GHZ


BIPOLAR AMPLIFIER (BPM)
NOISE PWR
CW PWR
NOMINAL DRIVE
POWER INPUT - dBm
26.0
27.0
28.0
29.0
OUTPUT POWER (dBm)
40
35
30
NOISE POWER - dBm/100 kHz
-75
-80
-85
-90

EXTENDED ANTENNA ARRAY TESTS

C

This section of the Test Plan covers the performance of the Dual Polarized Antenna at the Sub-Assembly Level. These tests were performed on the Outdoor Antenna Test Range. Each Array (RCVR & Xmit) was fed from a passive corporate feed. The tests performed were gain, sidelobes, beamwidth, and balun VSWR.

Each Antenna layer (Dipole Laminate) was tested individually as a single polarization using a flat aluminum sheet as the ground plane. The two laminates were assembled in a single aperature using the polarizer laminate as the transmit ground plane (maintaining the correct spacing between layers). Finally, the Dual Polarization was assembled in the final configuration (as delivered) and was evaluated with and without the radome (1/32" thick epoxy fiberglass G10).

Single & Dual Polarized Array Gain Comparison

Test Array

Freq GHz	Combiner Loss dB	Gain Including Combiner Loss* -dBi Array 1 Single Pol	Array 1 Dual Pol (Tx)	Array 2 Single Pol	Array 2 Dual Pol (Rx)
4.40	.97	30.7	28.5	31.3	29.1
4.50			31.0	31.2	29.6
4.55	1.02	30.8			
4.6			30.7	31.95	29.8
4.7	1.07	30.2	30.8	31.65	29.0
4.8			31.3	31.4	29.9
4.85	1.15	29.6			
4.9			30.7	31.4	30.5
5.0	1.22	29.5	29.2	31.05	29.9

* 4:1 Power Step Taper

Rx = Bottom Array, Tx = Top Array - as delivered

Test Array Sidelobe Comparison

Single and Dual Polarization

Frequency GHz	Maximum Sidelobe* -dB			
	Array 1		Array 2	
	Single	Dual (Tx)	Single	Dual (Rx)
4.40	15.2	15.4	16.0	14.6
4.55	15.0	15.9	16.2	16.0
4.70	15.3	14.6	16.0	14.0
4.85	13.5	15.3	15.0	14.0
5.00	14.9	14.6	14.8	15.5

*E, H and Intercadinal Planes; tested with combiner providing 4:1 step power taper

Rx = Bottom Array   Tx = Top Array

Test Array Beamwidth Comparison

Single and Dual Polarization

Frequency GHz	Array 1 Single	Array 1 Dual (Tx)	Array 2 Single	Array 2 Dual (Rx)
	Maximum Beamwidth * - Degrees			
4.40	3.85	3.85	3.78	3.70
4.55	4.00	3.60	3.66	3.60
4.70	3.83	3.50	3.50	3.55
4.85	3.83	3.40	3.30	3.40
5.00	3.67	3.30	3.20	3.30

*E, H Planes; Tested with 4:1 Power Step Taper Combiner

Rx = Bottom Array, Tx = Top Array - as delivered

Test Array VSWR Comparison

Single and Dual Polarization

Maximum VSWR: 4.4 to 5.0 GHz

Sub Array No.	Array 1 Single	Array 1 Dual (Tx)	Array 2 Single	Array 2 Dual (Rx)
1	1.47	1.50	1.37	1.65
2	1.40	1.58	1.39	1.83
3	1.50	1.63	1.50	1.89
4	1.55	1.57	1.60	1.84
5	1.63	1.85	1.80	2.14
6	1.65	1.82	1.70	2.10
Combined				1.91

Rx = Bottom Array, Tx = Top Array - as delivered

<u>Radome Effects</u>: The introduction of an epoxy fiber glass cover to the array face, as a radome, resulted in the following effects on performance:

Frequency GHz	Gain (Tx)		Sidelobes (E Plane, Tx)	
	No Radome dBi	Radome dBi	No Radome dB	Radome dB
4.40	29.6	29.6	15.0	14.8
4.70	30.3	30.3	14.9	14.3
5.00	30.9	30.9	14.9	14.4

These tests were done with the final array assembly.

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